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Simulation and Experimental Results of Low Noise SMPS System using Forward Converter

P. Vijaya Kumar[1] S. Rama Reddy[2]

Abstract–Simulation and Implementation of DC-DC converter side in SMPS system is discussed in this paper. A forward type soft switching DC-DC converter topology with neutral point inductor connected Auxiliary resonant snubber (NPC-ARS) circuit is presented in this paper for the switching mode power supply applications. Its circuit operation and its performance characteristics of the forward type soft switching DC-DC converter are described and the simulation and experimental results are presented.

Keywords- Forward type DC-DC converter, Zero voltage soft switching, Zero current soft switching, neutral point inductor connected Auxiliary resonant snubber (NPC-ARS) circuit.

I. INTRODUCTION

In recent years, the switching mode power supply (SMPS) system have been achieved with high power density and high performances by using power semiconductor devices such as IGBT, MOS-FET and SiC. However, using the switching power semiconductor in the SMPS system, the problem of the switching loss and EMI/RFI noises have been closed up. This course produced the EMC limitation like the International Special Committee on Radio Interference (CISPR) and the harmonics limitation like the International Electro technical Commission (IEC). For keeping up with the limitation, the SMPS system must add its system to the noise filter and the metal and magnetic component shield for the EMI/RFI noises and to the PFC converter circuit and the large input filter for the input harmonic current. On the other hand, the power semiconductor device technology development can achieve the high frequency switching operation in the SMPS system.

The increase of the switching losses has been occurred by this high frequency switching operation. Of course, the inductor and transformer size have been reduced by the high frequency switching, while the size of cooling fan could be huge because of the increase of the switching losses. Our research target is to reduce the EMI/RFI noises and the switching losses in the SMPS system by only one method. The solution method is the soft switching technique. Using LC resonant phenomenon, this technique can minimize the switching power losses of the power semiconductor devices, and reduce their electrical dynamic and peak stresses, voltage and current surge-related EMI/RFI noises under high frequency switching strategy.

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[1] Jawaharlal Nehru Technological University Jerusalem College of Engineering Hyderabad, India, E-mail: dvvijayaharini@rediffmail.com
[2]Electrical and Electronics Department, Jerusalem College of Engineering, Chennai India, E-mail: srr_victory@yahoomail.com

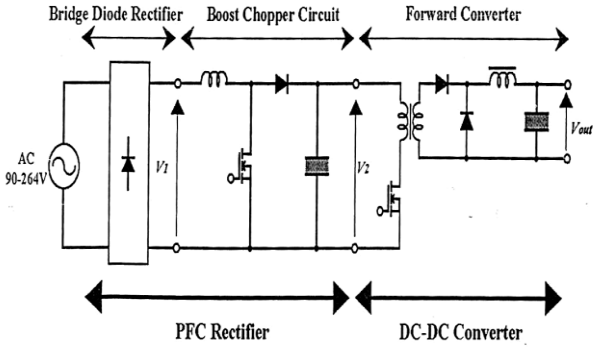

Fig.1.a: SMPS configuration of research target.

Thus, a new conceptual circuit configuration of the advanced forward type soft switching DC - DC converter which has the neutral point inductor connected auxiliary resonant snubber (NPC-ARS) circuit is presented in this paper with its operating principle in steady state. In addition, its fundamental operation and its performance characteristics of the proposed forward type soft switching DC-DC converter treated here are evaluated on the basis of experimental results. A New Controller scheme for Photo voltaics power generation system is presented in [1]. The design and implementation of an adaptive tuning system based on desired phase margin for digitally controlled DC to DC Converters is given in [2]. Integration of frequency response measurement capabilities in digital controllers for DC to DC Converters is given in [3]. A New single stage, single phase, full bridge converter is presented in [4]. The Electronic ballast control IC with digital phase control and lamp current regulation is given in [5]. A New soft-switched PFC Boost rectifier/inverter is presented in [6]. Design of Single-Inductor Multiple-Output DC-DC Buck Converters is presented in [7]. Boost Converter with Improved Performance through RHP Zero Elimination is given by [8]. High-efficiency dc-dc converter with high voltage gain and reduced switch stress is given in [9]. Snubber design for noise reduction is given in [10].Comparison of active clamp ZVT techniques applied to tapped inductor DC-DC converter is given in [11].The multiple output AC/DC Converter with an internal DC UPS is given in [12].The Bi-directional isolated DC-DC Converter for next generation power distribution –comparison of converters using Si and Sic devices is given in [13]. The above literature does not deal with embedded implementation of SMPS System employing forward converter. This work aims to implement SMPS System using low cost embedded Controller.

II. NOVEL FORWARD TYPE SOFT SWITCHING DC-DC CONVERTER

The typical switching mode power supply circuit

configuration of our research target is shown in Fig.1.a. We have modified the part of DC-DC converter to achieve the complete soft switching operation in active power semiconductor devices of the forward converter. Fig.1.b shows the schematic configuration of the modified forward type soft switching DC-DC converter with a neutral point inductor connected auxiliary resonant snubber (NPC-ARS) circuit. The proposed NPC-ARS circuit consists of an active power semiconductor devices; S_a, a resonant capacitor C_{rl}, two power diode D_{a1} and D_{a2}. Using this NPC-ARS circuit, the zero voltage soft switching (ZVS) turn off or the zero current soft switching (ZCS) turn on can be achieved in main switching device S_1 and ZCS turn on and turn off be in auxiliary switch S_a. So that, the switching losses in each active power semiconductor device will be zero completely.

III. Operation Principle of NPC-ARS Circuit

The operation principle of the proposed forward type soft switching DC-DC converter with the NPC-ARS circuit is illustrated in Fig.1.c. The conventional forward type DC-DC converter operates only two circuit condition modes which are described in Fig.1.c as the steady state mode on and off. On the other hand, there are 4 modes in case of the proposed one as depicted in Fig.1.c. The operating principle of the proposed forward type soft switching DC-DC converter is described as follows:

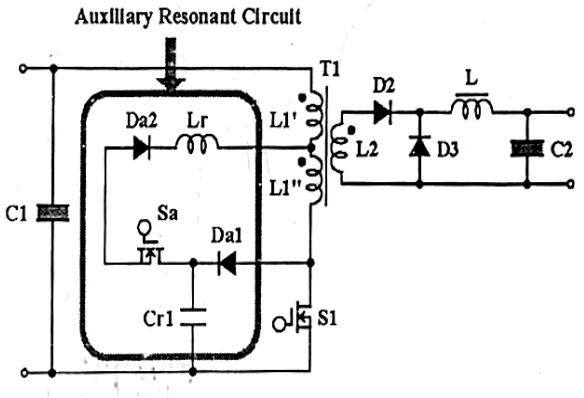

Fig.1.b: Forward type soft switching DC-DC converter with a neutral point inductor connected auxiliary resonant snubber (NPC-ARS) circuit.

Steady State Mode ON: In this state, the transformer current flows through the main active power semiconductor device S_1 and the primary energy conducts to secondary side of transformer. If the main active power semiconductor device S_1 is turned off, the operation mode changes to the next circuit condition mode, Commutation Mode 1.

Commutation Mode 1: The energy in the leakage inductance of transformer T_1 is flowing through the resonant capacitor C_{rl} by turned main active power semiconductor devices S_1 off. When the leakage inductance current reach zero, the operation mode changes to the next steady state mode, Steady State Mode off.

Steady State Mode OFF: The energy in the primary side of transformer is broken off the secondary side in this circuit condition mode. If the main active power semiconductor device S_1 and auxiliary active power semiconductor device S_a are turned on the operation mode changes to the next circuit condition mode, Commutation Mode 2.

Commutation Mode 2: In this mode, the active power semiconductor devices S_1 and S_a can be achieved the complete ZCS transition by the leakage inductance and auxiliary resonant inductor L_r. The energy in the primary side of transformer T_1 is conducted to the secondary side. Furthermore, the energy in the resonant capacitor C_{rl} flow to the secondary side of the transformer through the transformer T_1.When the voltage of the resonant capacitor C_{rl} reaches zero, the operation mode is changed to the first circuit condition mode, Steady State Mode on.

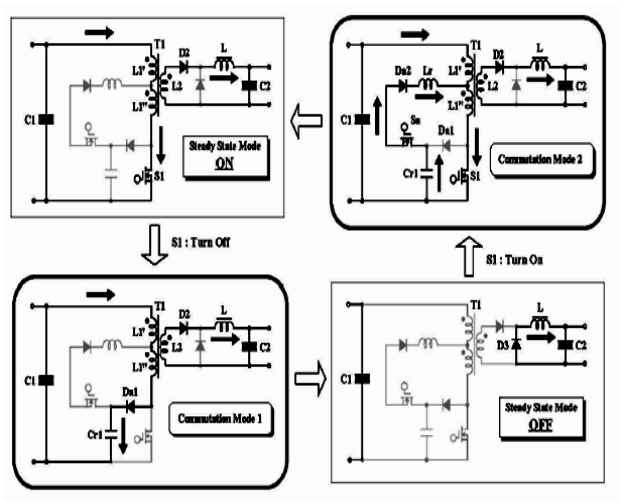

Fig.1.c: Equivalent circuit for each operation stage of the proposed forward type soft switching DC-DC converter with the NPC-ARS circuit.

IV. Mathematical Design for NPC-ARS Circuit

When the main switch *M1* is turned on at zero current as shown in Fig.3.g.input dc gets applied to the primary winding and simultaneously a scaled voltage appears across the transformer secondary. When the main switch *M1* is turned off at zero voltage as shown in Fig.3.g.The leakage inductance of a transformer and a voltage stress on the main switch is stored in the capacitor *Cr1* by the diode Da1and takes a path through the capacitor *C1* and to the transformer *L1′* up to the leakage inductance current reaches zero. The stored energy of the Capacitor *Cr1* is freewheels when the main and auxiliary switches are turned on at zero current.

The assumptions for the NPC-ARS auxiliary switch in the forward converter are:

Frequency f = 100 kHz, ΔI = 2.5, and R = 100 Ω. By using the relation 1- $\delta = V_i / V_o$, we get δ = 0.5.

By use the formula $L = V_i \ \delta / f \ \Delta I$, we get L=200 mH and

by the relationship $C = \delta / 2 f_r$, we get C = 250 µF and the voltage transformer ratio $V_o / V_i = K$, as by using this relationship we get the value of K=0.21.

The transformer primary voltage $E_1 = 4.44 * N_1 * \Phi * f$. By solving the equation to get the value of N_1 = 4.5, and by the equation $N_2 = (E_2 / E_1) N_1$ to get the value of N_2 = 9.

V. Simulation Results

The SMPS system is modelled and simulated using the blocks of MATLAB SIMULINK. The SMPS system using conventional boost and forward converters is shown in Fig.2.a. Diode rectifier with capacitor filter was represented as a DC source at the input. The current and voltage waveforms of *S2* are shown in Fig.2.b. The voltage across the primary of the transformer is shown in Fig.2.c. The voltage across the secondary of the transformer is Fig.2.d, the voltage across the diode d3 is shown in Fig.2.e.From the waveforms it can be seen that the output contains noise.

Modified SMPS system using auxiliary switch in the forward converter is shown in Fig.3.a. The voltage and current waveform of *S2* are shown in Fig.3.b. Voltage across the primary of the transformer is shown in Fig.3.c. The voltage across the secondary of the transformer is shown in Fig.3.d. The voltage across the diode *D3* is shown in Fig.3.e. The pulse and voltage across the switch *M2* is shown in Fig.3.f. The pulse and voltage across the switch *M1* is shown in Fig.3.g. The Current across the inductor *L1* is shown in Fig.3.h. The voltage across the capacitor *C2* is shown in Fig.3.i. From the above waveforms it can be seen that the output is free from noise.

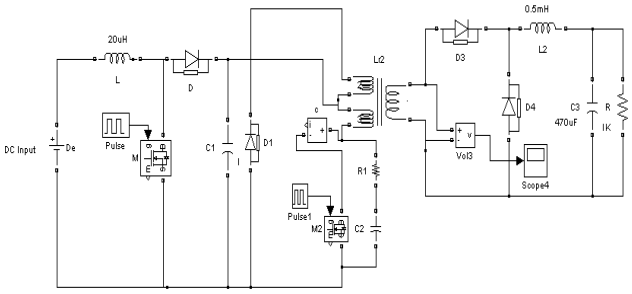

Fig.2.a: Conventional Boost & forward converter.

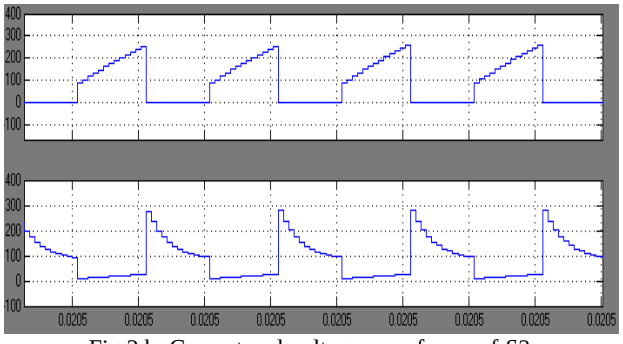

Fig.2.b: Current and voltage waveforms of *S2*.

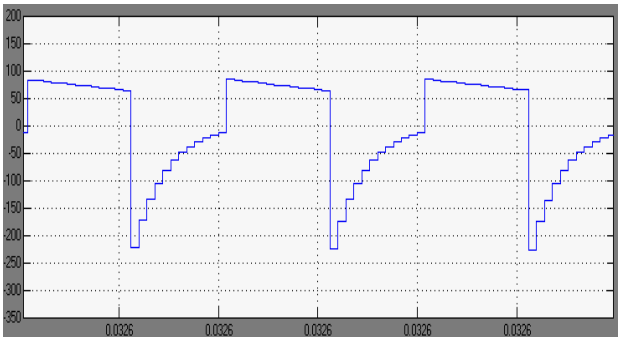

Fig. 2.c: Transformer primary voltage.

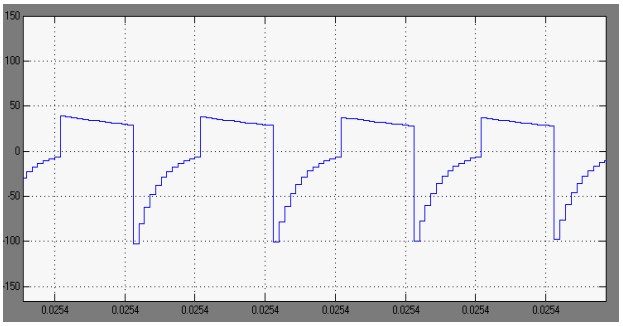

Fig.2.d: Transformer secondary voltage.

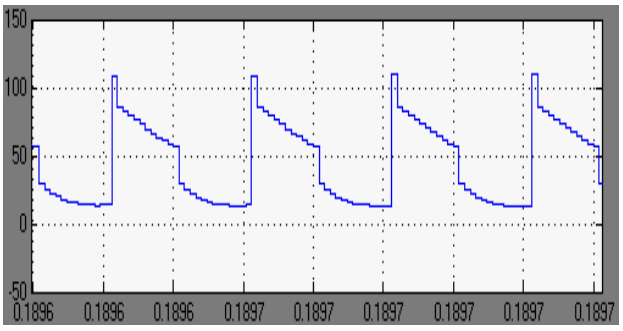

Fig.2.e: Voltage across diode *D3*.

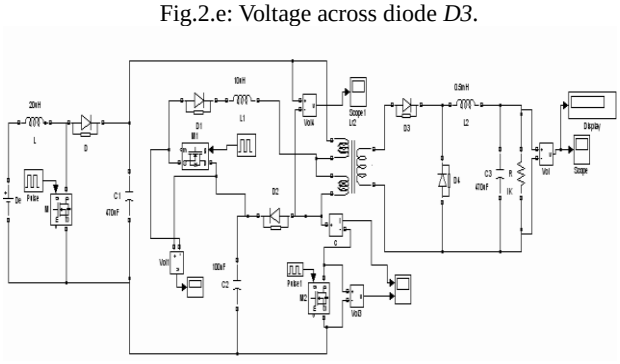

Fig.3.a: Modified SMPS system using auxiliary switch in the forward converter.

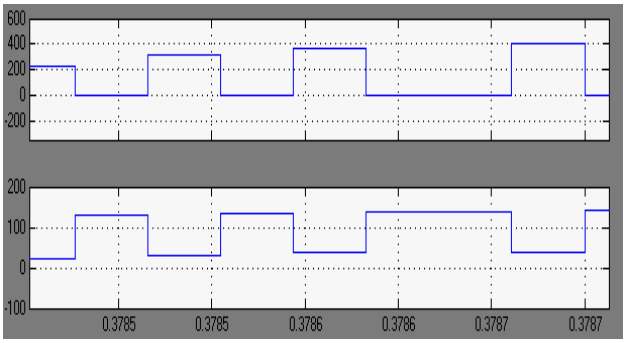

Fig.3.b: Current and voltage waveforms of S2.

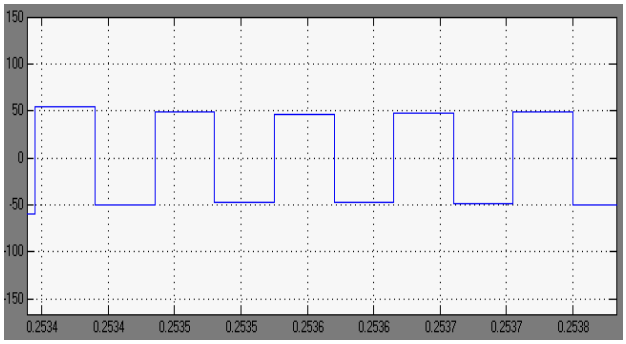

Fig.3.c: Transformer primary voltage.

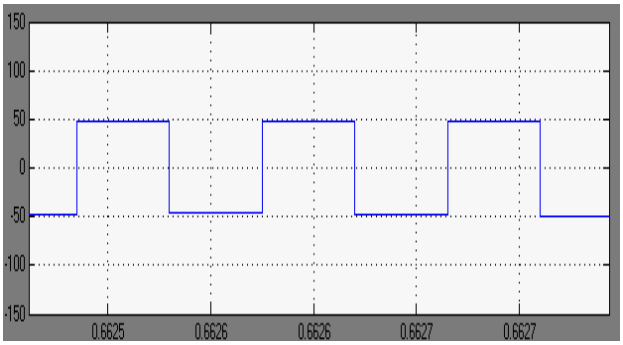

Fig.3.d: Transformer secondary voltage.

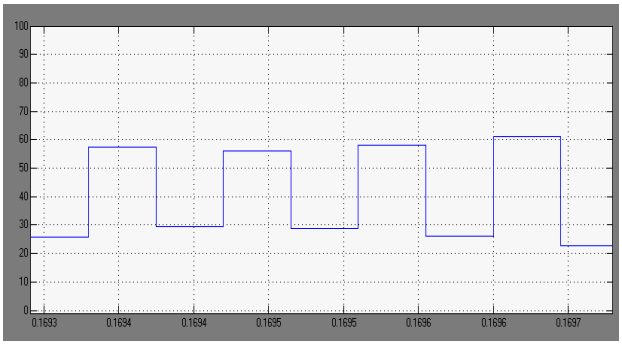

Fig.3.e: Voltage across diode D3.

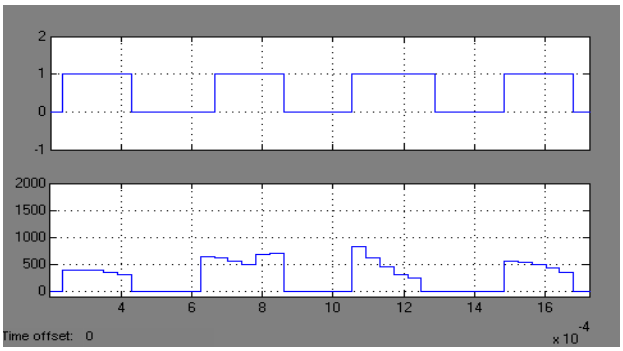

Fig.3.f: Pulse and voltage across the switch M2.

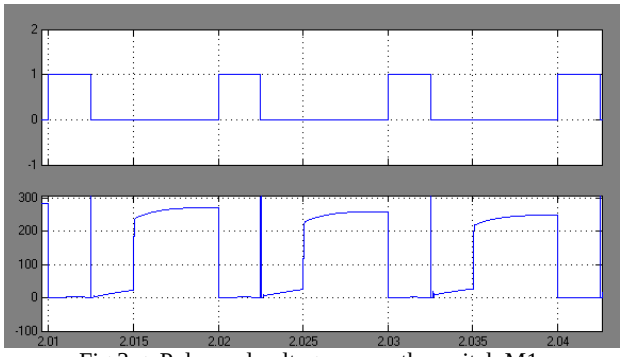

Fig.3.g: Pulse and voltage across the switch M1.

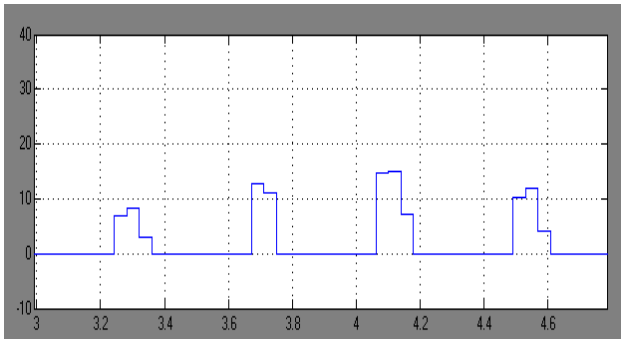

Fig.3.h: Current across the inductor L1.

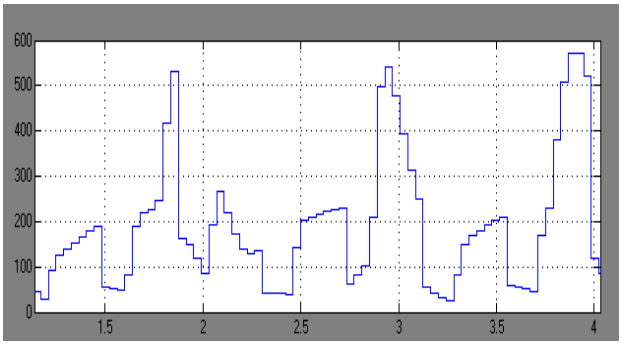

Fig.3.i: Voltage across the Capacitor C2.

VI. EXPERIMENTAL RESULTS

Low noise SMPS System with forward type soft switching DC-DC Converter with a neutral point inductor connected auxiliary resonant snubber circuit is designed and the hardware module is shown in Fig.4.a.The Atmel Microcontroller 89C2051 is used to generate the driving pulses for the thyristor S_a and S_1 as shown in the oscillogram of Fig.4.b and Fig.4.c.The Boost up driving pulses as shown in the oscillogram of Fig.4.d.

The transformer Primary voltages at the input with disturbances and the transformer secondary voltages at the output with disturbances as shown in the oscillogram of Fig.4.e. and Fig.4.f.The DC output voltage as shown in the oscillogram of Fig.4.g. The inductor current in NPC-ARS circuit is shown in Fig.4.h. The Capacitor voltage in NPC-ARS circuit is shown in Fig.4.i.The important circuit parameters of conventional circuit are indicated in TABLE 1. The circuit parameters in the proposed one are in TABLE 2. The experimental results are obtained for constant load.

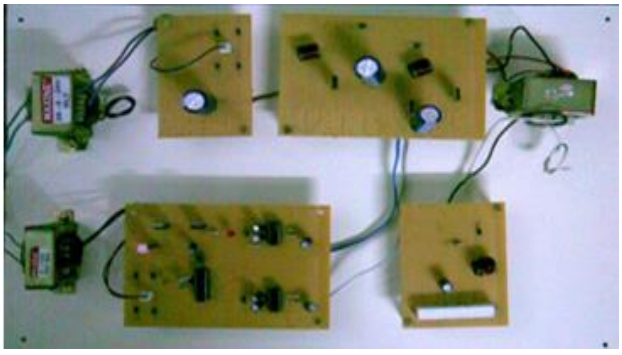

Fig.4.a: Hardware Module.

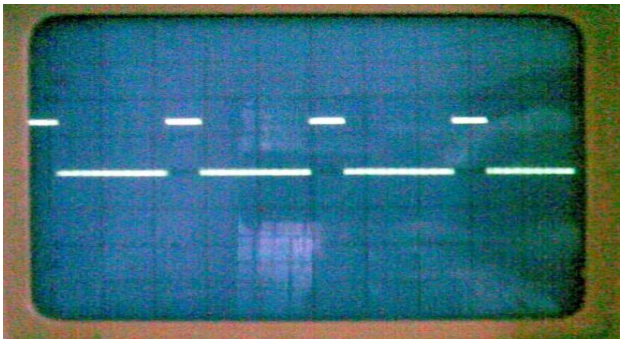

Fig.4.b: Driving Pulse of *Sa*.

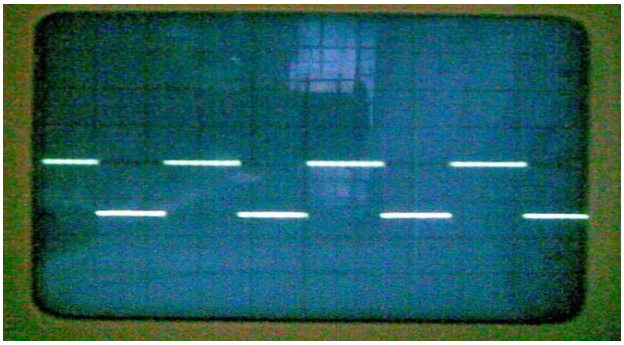

Fig.4.c: Driving Pulses of *S1*.

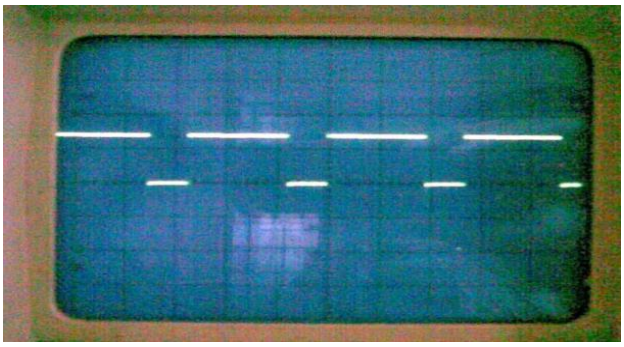

Fig.4.d: Driving Pulses of Boost Transistor.

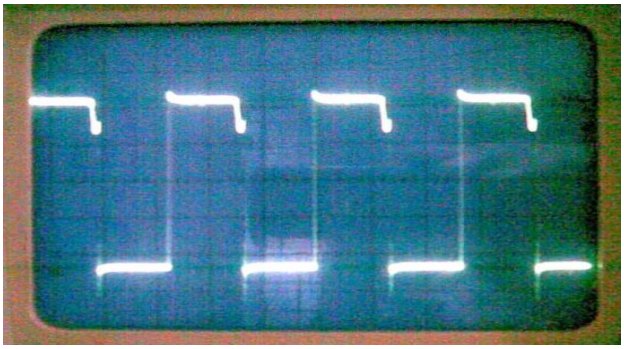

Fig.4.e: Transformer Primary Voltage.

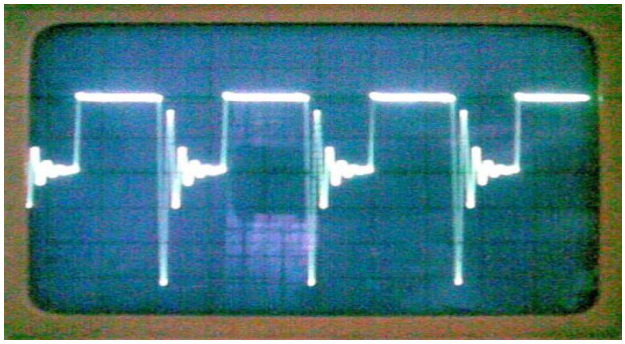

Fig.4.f: Transformer Secondary Voltage.

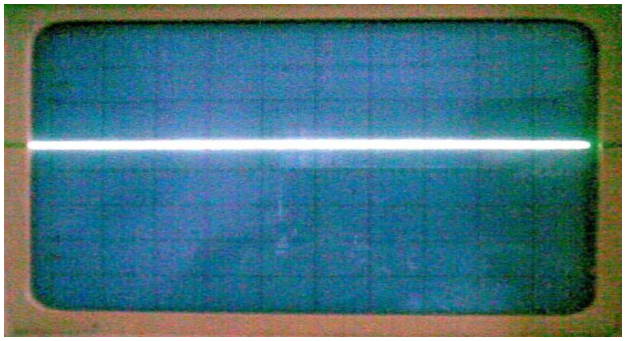

Fig.4.g: DC Output Voltage.

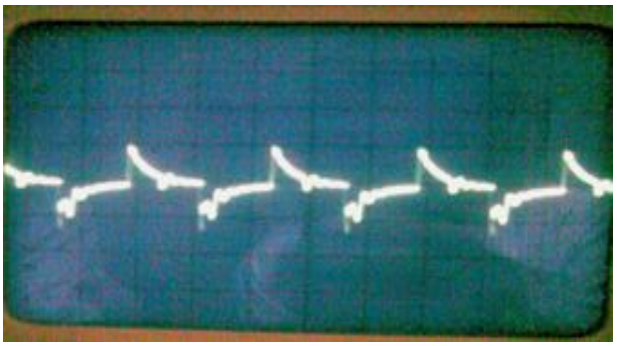

Fig.4.h: Inductor Current in NPC-ARS Circuit.

Fig.4.i: Capacitor Voltage in NPC-ARS Circuit.

Table 1: Circuit Parameters for Conventional Circuit

Parameters	Unit	Values and Items
Input Voltage	[V]	48
Output Voltage Vo	[V]	18
Switching frequency	[kHz]	30
Smoothing Capacitor *C1,C2*	[μf]/*V*	2200/63,100/63
Smoothing Inductor L	[*m*H]	27
Capacitance of Snubber circuit		1000 μF/63 V
Resistance of Snubber circuit		330 ohm/20W
Power MOSFET		IRF 840
Power Diode		IN4007

Table 2: Circuit Parameters for Proposed Circuit

Parameters	Unit	Values and Items
Input Voltage	[V]	48
Output Voltage *Vo*	[V]	18
Switching frequency	[kHz]	30
Smoothing Capacitor *C1,C2*	[μf]/V	2200/63,100/63
Smoothing Inductor L	[mH]	27
Inductance of NPC-ARS circuit	[μH]	10
Capacitance of NPC-ARS circuit	[*n*f]	100
Power MOSFET		IRF 840
Power Diode		IN4007

VII. Conclusion

Implementation of low noise SMPS System using forward converter with MATLAB-SIMULINK was done using microcontroller. Modified circuit configuration of forward type DC–DC converter with its working principle is presented in this paper. The conventional and modified SMPS systems are digitally simulated using Sim power systems. The simulation results and the experimental results are compared. The modified converter has reduced noise in the output. From the results, it is observed that the experimental results closely agree with the simulation results.

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Biographies

P.Vijayakumar received his Diploma in Electrical and Electronics Engineering from A.S.A Polytechnic, Tenkasi, affiliated to DOTE, Chennai, India in 1996 and B.E degree in Electronics and Communication Engineering from V.R.S College of Engineering and technology, Madras University, Chennai, India in 2002 and M.Tech degree in Power Electronics and Drives from Bharath Institute of Higher Education and Research, Bharath University, Chennai, India in 2005.Currently he is Pursuing Ph.D degree in Jawaharlal Nehru Technological University, Hyderabad, India. He has 9 years of teaching experience and 3 years of Industrial experience and he is a member of IEEE. His research area is on SMPS System.

S.RamaReddy received his M.E degree from College of Engineering, Anna University, Chennai, India in 1987.He received Ph.D degree in the area of Resonant Converters from College of Engineering, Anna University, Chennai, India in 1995.Presently he is working as Dean in Electrical and Electronics Department, Jerusalem College of Engineering, Chennai. He has worked in Tata Consulting Engineers and Anna University, Chennai, India. He is fellow member of Institution of Electronics and Telecommunication Engineers (India),

Life Member of Institution of Engineers (India), Member of ISTE, Member of CSI and Member of SPE, India. He has authored text books on Power Electronics, Electronic Circuits and Electromagnetic Fields. He has Published 30 research papers in reputed journals. His research areas are Power Electronic Converters, Drives and FACTS.

Single-Stage Solar Photovoltaic Array Fed Water Pumping System

Sonak Singh[1] Bhim Singh[2]

Abstract–The single stage solar photovoltaic (SPV) array fed water pumping system consists of a solar PV array, voltage source inverter (VSI) and an induction motor driven pump set. In this system, VSI performs maximum power tracking (MPP) from the solar PV array and also controls the speed of an induction motor using V/F control algorithm. The reference speed for V/F control is estimated by a new approach. The reference speed is estimated from two components, one from the dc-link voltage of VSI and other from the PV array power. The reference speed of the motor mainly depends on the PV array power and the tracking of maximum power, if variation occurs in the solar PV power then the reference speed of induction motor changes accordingly. The model of proposed system is developed in the MATLAB/Simulink and its simulated results have demonstrated the satisfactory performance in dynamic as well as in steady state operating conditions.

Keywords–solar PV panel, voltage source inverter, induction motor, pump set

I. INTRODUCTION

In Indian economy, GDP of agriculture is approximately 16%.According to the studies, India can contribute other countries not just itself in agricultural products but the output of agriculture products falls due to several factors. The main factor for agriculture products is the water [1]. Mainly rivers, canals, wells and monsoons water are used for the agriculture products. In India, 64% of cultivated land mainly depends on monsoons. Irrigation is important to reduce the dependence on monsoons in India. Diesel pump sets are used in India for irrigation but diesel pump-set has high maintenance cost and also creates pollution. The motor pump sets are also used for the irrigation where grid electricity is present but in India. Many rural areas are not so developed and the grid electricity is not present. So, the solar PV (Photo-Voltaic) array fed water pumping system can easily meet the irrigation problem easily [2]. Its maintenance cost is negligible and does not create pollution but its installation cost is high. Solar PV array fed water pumping system life span is observed approximately 25-30 years.

Solar PV water pumping systems are already in use in worldwide. Solar PV array fed dc motor driven pump sets are already in use. For extracting the maximum power, a dc-dc converter requires at output of solar PV array for this system. When the insolation varies a very small variation occurs in the output voltage of PV array but large variation occurs in the PV array current. The speed of the dc motor changed very less because the speed of the dc motor depends on the voltage but the large variation in load torque because it depends on the current [3,4]. Some authors have used lookup table in solar PV array fed dc motor pump set [5]-[7]. Carbon brushes are present in the dc motor which causes sparking inside the dc motor due to this loss in the dc motor are high and maintenance cost is high. So, the dc motor pump set cannot be used in mining and chemical industries.

Solar PV array fed induction motor driven pumps are also used but the efficiency of the low rating induction motor is less. So, high rating induction motor pump sets are mostly used for solar water pumping system. Such systems are of two types one is single-stage [8]-[12] and other is two-stage [13, 14]. In single stage, only VSI (Voltage Source Inverter) extracts the maximum power from SPV array and also controls the induction motor. In two stage system, a dc-dc converter is first stage and VSI is second stage. In two stage system, a dc-dc converter is used for MPPT of SPV array and VSI is used for the induction motor control. The two-stage system is used for higher power rating. Solar fed induction motor driven pumps are reliable and maintenance free and it can be used in any industry because of no sparking and less loss compared to the dc motor. Mainly two types of control of the induction motor are used for such systems as V/F control [8]-[10] and vector control [12]-[14]. Z-source inverters are also used for single stage solar water pumping system [11].

Solar PV array fed PM brushless DC motor is also used for this system [15]-[18]. DC source supplied to PM brushless DC motor via a VSI. The system requires dc-dc converter and VSI. This motor requires extra sensors for electronics control of the VSI. A PMBLDC motor is more efficient than an induction motor but it is more costly than an induction motor.

In this paper, a solar PV array fed induction motor driven pump is investigated in detail. This system is single-stage system, only an inverter performs both functions. One is MPPT of SPV array and controlling the speed of an induction motor. The reference speed of an induction motor for V/F control is estimated using a new approach. The reference speed in this control is estimated using two components one from the MPPT of SPV array and other from the SPV power. In this single-stage system, the dc-link voltage of VSI is floating. The system performance is demonstrating through simulated results.

II. PROPOSED SINGLE-STAGE SPV WATER PUMPING SYSTEM

Fig.1 shows the single-stage solar PV array fed water pumping system. The proposed system consists of three parts which are SPV array, VSI and an induction motor driven pump set. The proposed system requires only voltage and current sensors for MPPT of SPV array. In this

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[1] Department of Electrical Engineering, Indian Institute of Technology Delhi, Hauz Khas, New Delhi-110016. E-mail:sonak1989@gmail.com
[2] Department of Electrical Engineering, Indian Institute of Technology Delhi, Hauz Khas, New Delhi-110016. E-mail: bsingh@ee.iitd.ac.in

system, the SPV array is directly connected to the dc-link of the VSI and the control of this VSI performs both task, one is maximum power point tracking and other is controlling the speed of an induction motor driven pump.

III. DESIGN OF SINGLE-STAGE SPV WATER PUMPING SYSTEM

In the proposed system, a 5 hp (3.7 kW) pump driven by an induction motor is extracting the power from the solar PV array. For this pump, a 5.3 kW solar PV panel is selected because some losses are also present into the system.

A. Selection of DC Capacitor Voltage

In order to achieve proper dc-link voltage compensation, the minimum DC-link voltage of VSI must be greater than the phase voltage of the proposed system as [18],

$$V_{dc} = \frac{2\sqrt{2}V_{LL}}{\sqrt{3}} = \frac{2\sqrt{2}\times 415}{\sqrt{3}} = 677.7V \quad (1)$$

where V_{LL} is the line voltage of the induction motor. The estimated value of the V_{dc} from (1) is obtained as 677.7 V and it is selected as 700V.

B. Solar PV Panel Modeling

A solar PV panel consists of several solar cells in series or parallel to convert solar insolation into electricity. Here the PV panel system is designed to have peak power rating of 5.3 kW at 1000W/m^2.

The SPV array maximum rating used for proposed system is 5.3 kW. Each PV module has a rated power of 200 W, a rated current of 7.6 A, a rated voltage of 26.3 V, a short-circuit current of 8.21 A, and an open circuit voltage of 32.9V [19].

The active power generated by the SPV array is given as,

$$P_{maxM} = V_{mppM} * I_{mppM} \quad (2)$$

Maximum power of SPV array generally given as, P_{maxM} = (80% of V_{oc} * 90% of I_{sc}) thus I_{mppM} is 7.61A and V_{mppM} is 26.3V of each module. In order to get a DC-link voltage of 700V, PV array voltage at MPP should around 700V under different insolation conditions. MPP voltage should vary around 700V for irradiance variation from 1000W/m^2 to 200W/m^2 for proper operation of the voltage source inverter.

$$P_{max} = V_{mpp} * I_{mpp} = 700\times 7.6 = 5.3 \text{ kW} \quad (3)$$

From (3), a 5.3 kW power capacity is achieved.

The numbers of PV modules connected in series are as, N_s= 700/26.3=26.61 (27 selected)

The current rating required is as, I_{pv}=7.6A

Number of parallel strings is as, N_p=7.5/7.6 = 1

C. Design of DC-Link Capacitor

The energy conservation principle is used to estimate the value of DC capacitor [20],

$$\frac{1}{2}C_d\left[V_{dc}^2 - V_{dc1}^2\right] = 3aVIt \quad (4)$$

$$\Rightarrow \frac{1}{2}C_d\left[700^2 - 680^2\right] = 3\times 1.2\times 239.6\times 7.5\times 0.01 watts$$

It results in the dc link capacitance as, C_d = 4687.82µF.

where V_{dc} is the reference DC-link voltage and V_{dc1} is the minimum DC-link voltage, a is the overloading factor of VSI, V is the motor phase voltage, I is the motor phase current, and t is the time by which the DC-link capacitor

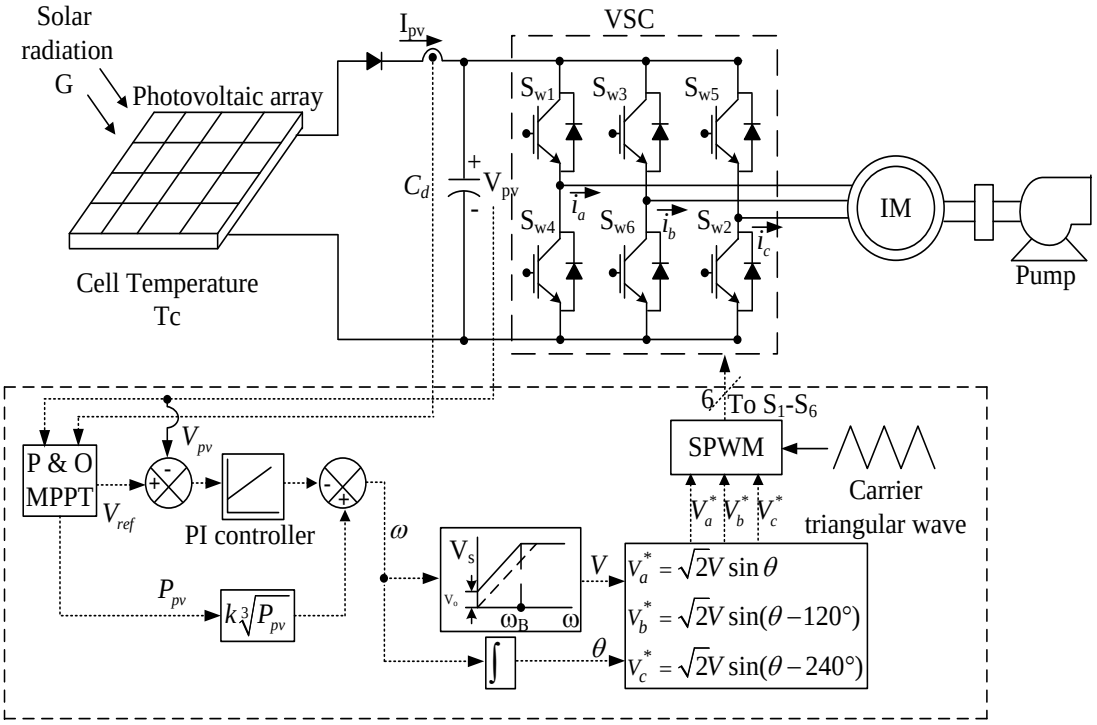


Fig.1 Proposed system of Solar Photovoltaic array Fed Water Pumping System

is to be charged. It results in the value of a dc capacitor C_d of the order of 4687.82 μF and it is selected as 5000 μF.

IV. CONTROL ALGORITHM FOR PROPOSED SPV WATER PUMPING SYSTEM

Fig.1 shows the proposed single-stage SPV water pumping system. The V/F control is used to control the speed of an induction motor. The proposed system control scheme is shown in Fig.1.

A. Maximum Power Point Tracking

Several MPPT algorithms are used to extract the maximum power from the solar PV array [21]. The P&O (Perturb & Observe) method is used in this system. This algorithm has been mainly used because its easy implementation and reduced complexity. Fig. 2 shows the P&O control algorithm.

In this method, voltage (dc-link voltage) and current of SPV array are sensed and are fed to the controller in which the change in sensed DC-link and PV power are estimated. The algorithm periodically tracks the MPP and operates by increasing or decreasing the reference dc-link voltage. From flow-chart shown in Fig.2, it can be observed that at first the present samples for $V_{pv}(k)$ and $I_{pv}(k)$ are sensed than $P_{pv}(k)$ is generated by multiplying the $V_{pv}(k)$ and $I_{pv}(k)$. The present and one past sample set $P_{pv}(k-1)$, $V_{pv}(k-1)$ are used for calculation of ΔP_{pv} and ΔV_{pv}. The governing equations used for the P&O MPPT at one insolation level are as,

$\Delta P_{pv}=0$ and $\Delta V_{pv}=0$, at MPP (5a)

$\Delta P_{pv}>0$ and $\Delta V_{pv}>0$, (5b)
Left of MPP on P_{pv} versus V_{pv} curve

$\Delta P_{pv}<0$ and $\Delta V_{pv}<0$, (5c)
Right of MPP on P_{pv} versus V_{pv} curve

The reference voltage is adjusted using eq. (6). The variation in reference voltage according to governing equations is as,

if $\Delta P_{pv}=0$ and $\Delta V_{pv}=0$

$V_{refnew}=V_{refold,}$ (6a)

if $\Delta P_{pv}>0$ and $\Delta V_{pv}>0$ or $\Delta P_{pv}<0$ and $\Delta V_{pv}<0$

$V_{refnew}=V_{refold}+step,$ (6b)

if $\Delta P_{pv}>0$ and $\Delta V_{pv}<0$ or $\Delta P_{pv}<0$ and $\Delta V_{pv}>0$

$V_{refnew}=V_{refold}-step,$ (6c)

Finally the values of $V_{pv}(k-1)$ and $I_{pv}(k-1)$ are updated for next iteration. V_{refnew} is assigned as output. The control of V_{ref} ensures that SPV array is operating at maximum power point.

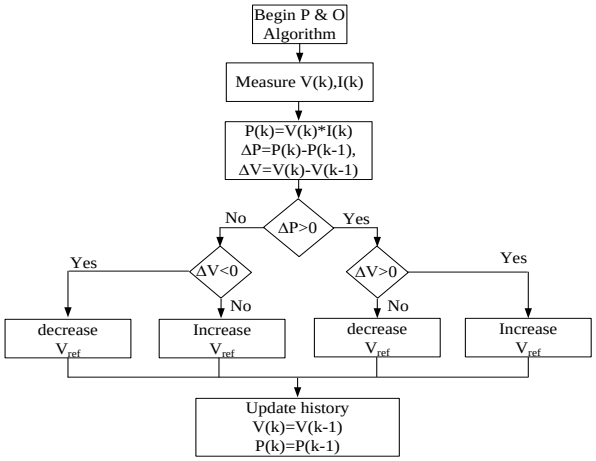


Fig.2 Flow chart of P & O algorithm

B. Control of an Induction Motor

In this system, the speed of an induction motor is controlled by the V/F control. The V/F control of an induction motor driven pump does not use any sensors for the motor control. It's an open loop control. In this system, the reference speed of the motor is calculated by the MPPT algorithm and solar PV array power. In this control, the speed control of the drive is directly controlled by a voltage source inverter.

1) Estimation of Reference Speed

The pump model correlation between the torque and speed is approximated as,

$$T = a_1 + a_2\omega^2 \tag{7}$$

where, a_1, a_2 are the constants of the pump, T and ω are the torque and the speed of the pump respectively. Pump characteristics analogous to the flow rate and head of the pump. Manufacturer gives information about the hydraulic pumps. According to the affinity law states that power is proportional to the cube of the speed ω at which the centrifugal pump is running [12].

In this system, affinity law is used to estimate the one component of reference speed. So, the motor operates under the solar insolation variation and it determines the centrifugal pump flow rate. The one component of reference speed corresponding to the PV power is given as [12],

$$\omega_1 = K\sqrt[3]{P_{pv}} \tag{8}$$

where K is constant for converting the PV array power into speed and P_{pv} is the power of PV array.

The dc-link voltage controller is used to estimate the second component of the reference speed. In this system, the actual dc-link voltage (V_{dc}) compares with the reference dc-link voltage (V_{dc}^*) results in a voltage error is given as

$$V_{dcl(n)} = V^*_{dc(n)} - V_{dc(n)} \tag{9}$$

This error signal is passed through the voltage controller, and the output speed is given as,

$$\omega_{2(n)} = \omega_{2(n-1)} + K_{pdc}\left\{V_{dcl(n)} - V_{dcl(n-1)}\right\} + K_{idc}V_{dcl(n)} \quad (10)$$

where K_{pdc} and K_{idc} are the proportional and integral gains of the dc-link voltage PI controller. The losses of the system account the output of this PI controller.
The reference speed for an induction motor drive is given as,

$$\omega_r^* = \omega_1 - \omega_2 \quad (11)$$

where ω_r^* is the reference speed and ω_1 is used from (8) and ω_2 is used from (10).

2) V/F Control of an Induction Motor

In industry, the V/F control of an induction motor is commonly used for speed control. In this control, the air gap flux of the motor remains constant so that the ratio of voltage and frequency are changed proportionately. In this, no sensed signals are required for the control of the induction motor. Fig.1 shows the control scheme of V/f speed control.

The reference speed ω_r^* is the control parameter for V/F control. The phase voltage V of the induction motor changes, when the reference speed of an induction motor is controlled up-to base speed. The phase voltage of the induction motor remains at its rated value, if the reference speed is greater than the base speed. The power consumption in variable speed control drive is reduced when operated in fully open loop control. Angle θ is generating by integrating the ω signal, and the using of angle θ, reference voltage (v_a^*, v_b^* and v_c^*) signals are generated as shown in Fig.1. The reference voltages signals are comparing with the carrier wave and the switching PWM signals are generated for the VSI [8]-[10].

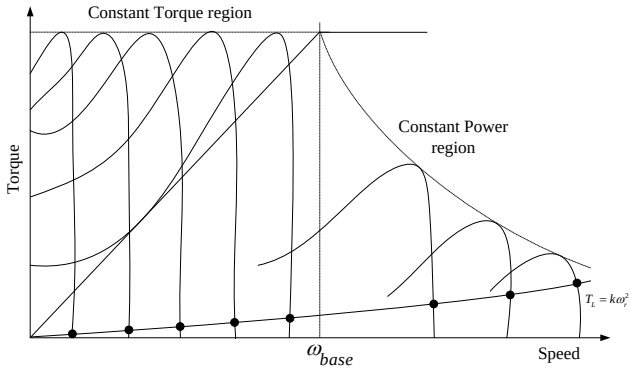


Fig.3 Torque -speed curve showing effect of frequency variation. Supply voltage and load torque changes

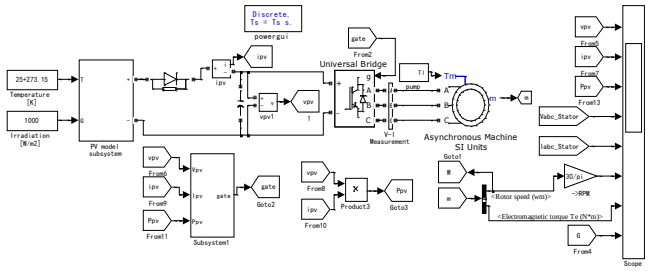
The steady-state performance of an induction motor drive on a torque-speed curve with a pump-type load ($T_L = K\omega_r^2$) is shown in Fig 3. The points are indicated that as the speed is gradually increased, the torque is proportional to the speed square. If the reference speed of induction motor changes than the operating point shifts to another torque-speed curve correspondingly the phase voltage of an induction motor increases up to base speed after that it remains constant.

V. MODELING AND SIMULATION OF PROPOSED SPV WATER PUMPING SYSTEM

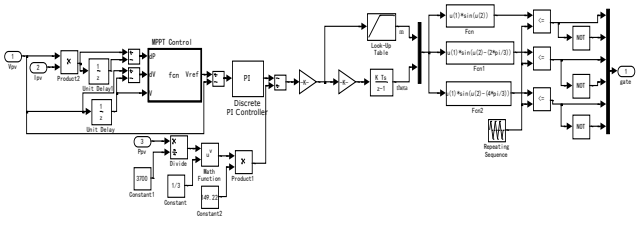
The performance of proposed single-stage solar photovoltaic array fed water pumping system is simulated using the developed model in MATLAB/Simulink platform as shown in Fig.4 (a).The developed Simulink model for generating reference speed using SPV power and MPPT voltage controller is shown in Fig.4 (b). The rating of the induction motor considered for this simulation is a 5 hp (3.7 kW), 415V and 50 Hz.

VI. RESULTS AND DISCUSSION

A solar PV water pumping system is modeled using MATLAB\Simulink. The proposed SPV water pumping system not only extracting the maximum power from the PV array and also generates different reference speeds at different insolation level. To demonstrate this feature the results are shown in Figs.5-6 and following observations are made based on these results.



(a)



(b)

Fig.4 single stage solar water pumping system (a) MATLAB model, (b) control model

A.Performance for Maximum Power Tracking

Fig. 5 shows the dynamic response of MPPT of SPV array. In Fig.5, V_{pv} starts from 821 V because dc-link capacitor of VSI already charged with open circuit voltage of PV array, when the MPPT P&O algorithm is enabled then the voltage reduces and the current increases for tracking the maximum power point. Fig.5 shows the steady state response of MPPT of SPV array. Fig.6 shows the dynamic and steady state performances of maximum power point tracking at different solar insolation level.

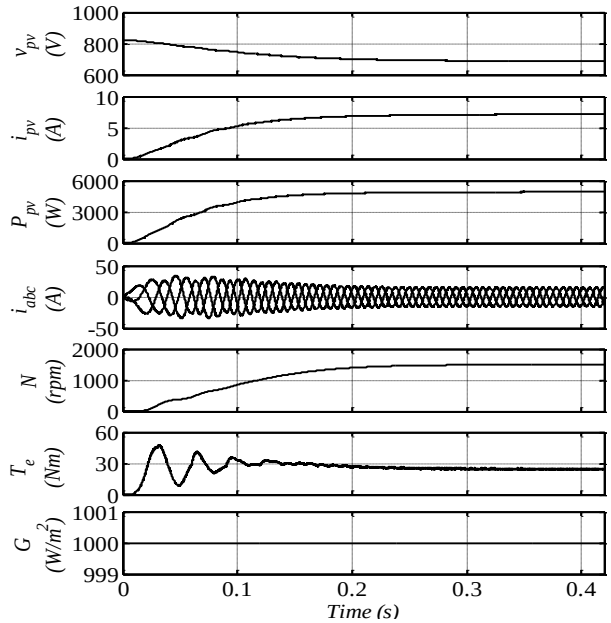


Fig.5 Dynamic and steady performances of PV array fed water pumping system at 1000W/m^2

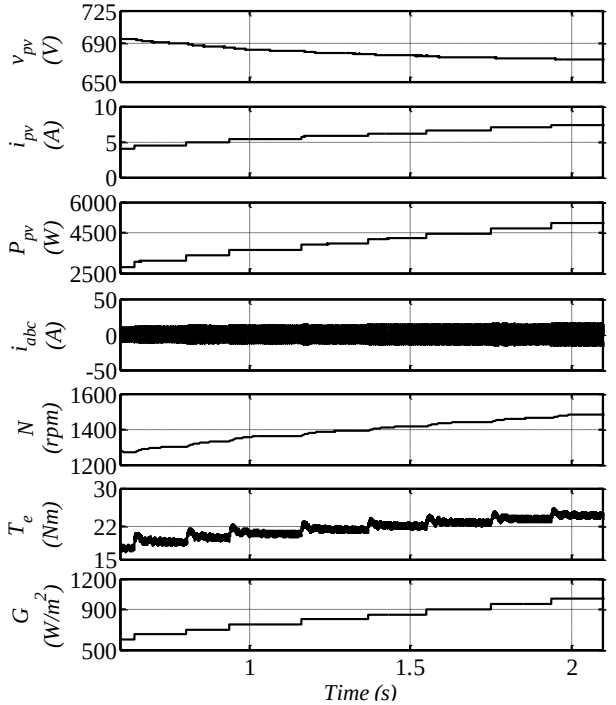


Fig.6 Effect of solar insolation level on the performance of SPV array fed pump

B. Performance of Solar PV Pumping System

The speed of an induction motor speed is controlled by the V/F control and the reference speed for this control is decided by the PV power (P_{MPPT}) or the radiation (G) and the MPPT algorithm. Fig.5 shows that the P&O algorithm is working well for MPPT of the SPV array. Fig.5 also shows the dynamics of SPV water pumping system at 1000*W/m*^{2}. In this system, the solar radiation of 1000*W/m*^{2} is generated to study the performance of the proposed model, which sets the reference speed corresponding to the solar PV array power and dc-link voltage. Fig.5 also shows the steady state performance of SPV water pumping system at 1000*W/m*^{2}. Fig.6 shows the results at different insolation levels. It shows that the speed changes, when the insolation changes. In this system, solar radiation varies between 200W/m^2 to 1000W/m^2 to study the performance of this control. According to the radiation, the reference speed changes and the load torque also changes because the load torque depends on the speed of the motor for pump load. Table-I shows the simulation results different reference speed, PV power and PV current at different insolation. From these results, it is observed that the proposed single stage SPV fed water pumping system works satisfactorily over the wide range of solar insolation level.

VII. CONCLUSION

The proposed single-stage solar PV water pumping system using V/F control has controlled the speed of an induction motor drive. A new approach has been used for generating reference speed for the V/F control of an induction motor which has been utilized by controlling the voltage at dc bus and the pump affinity law is used to achieve the different speeds. The reference speed has been generated by the difference of speed generated by solar PV power and MPPT algorithm. The reference speed of the induction motor has changed during varying atmospheric conditions for extracting the maximum power from solar PV array. The maximum power extracted by perturbs and observe algorithm optimizes the energy transfer towards the motor. The P&O technique reaches the maximum power without oscillations. In this system, dc-link voltage of VSI is floating because at the maximum power point voltage changes at different insolation level for MPPT. The simulation results of the controller shows satisfactory performance under steady state as well as dynamic conditions.

APPENDIX

A. Solar PV Array Data

V_{mppt} = 700V, I_{mppt} = 7.6A, V_{oc} = 821V,
I_{sc} = 8.21A.

B. Motor Characteristics

P = 3.7W, V = 415V, N = 1425rpm, f=50Hz,
R_s=1.7Ω, L_{ls}=0.00967H, R_r=1.85Ω,
L_{lr}=0.00967H, L_o=0.210527H, J=0.02428kg/m^2

C. Pump Characteristics

$T=a_1+a_2\omega^2$, a_1=-35.34, $a_2= 2.7\times10^{-03}$

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BIOGRAPHIES

Sonak Singh received his B.Tech. in Electrical Engineering from SBSCET, Ferozepur, Punjab. He has done his M.Tech in Power Electronics, Electrical Machines and Drives from IIT Delhi. His interest includes solar energy systems, electrical machines and drives.

Bhim Singh received his BE Electrical Engineering from University of Roorkee, in 1977, MTech in 1979 and PhD in 1983 from IIT Delhi, India. In 1983, he joined Department of Electrical Engineering, University of Roorkee, as a Lecturer. He became a Reader there in 1988. In December 1990, he joined Electrical Engineering Department, IIT Delhi, as an Assistant Professor. He became an Associate Professor in 1994 and a Professor in 1997. His areas of interest include power electronics, drives, renewable energy systems and power quality. He is a Fellow of INAE, INSA, NASI, IASc, TWAS, IEEE, IET, IEI, IETE.

Electronic Commutation of DC Motor

Rajendra Bhamu [1]

Abstract–This paper focuses on the design and implementation of electronically commutated DC MOTOR. The electronic MOSFET is used as switch. For a P pole machine in lap & wave winding configuration coils can be wound for no. of parallel path. The stator consists of slots for armature winding and the rotor has dc field winding or permanent magnet. The MOSFET switch is triggered in a specific pattern according to connection with coil using microcontroller. The speed control of the motor is very flexible. The motor can run in linear motion, discrete motion, exponential motion, linearly increasing & linearly decreasing motion. Reversal of direction of rotation is easy. Motor can run in desired speed range from minimum speed up to maximum speed. Winding of the motor is suitability connected according to V- I rating of source like lap or wave configuration.

Keywords–Electronic commutation, MOSFET switch, microcontroller triggering, A-D converter, Flexible speed control

I. INTRODUCTION

Electric motors are one the most essential components and the driving force of industry today. It is estimated that more than five billion motors are built worldwide every year. In general, there are two types of motors namely ac and dc. The ac motors are usually less expensive, rugged and have low maintenance but hard to control, on the other hand the dc motors are more expensive, but highly controllable. The conventional dc motors are highly efficient and their characteristics make them suitable for use in different applications. However, one of their drawbacks is the need for a commutator and brushes, which are subject to ware and require maintenance. When the task of commutator and brushes are replaced by solid-state switches, maintenance-free motors were realized and the new motor called brushless dc motors emerged. The commutation problem of dc motor limits their use. Brushless dc motors (BLDC) are one of the motor types rapidly gaining popularity. The construction of modern BLCD motors is very similar to the ac motor, known as the permanent magnet synchronous motor. BLDC motors come in single-phase [1], 2-phase and three-phase configurations [2]. Out of these, the 3-phase motors are the most popular and widely used. Much research has been done on the modeling and analysis of Brushless DC motor and many application note has been prepared by industries regarding working of BLDC motor [3],[5-11].

This paper represents exact electronic commutation of dc motor. In electronic commutation scheme for the commutation process reversal of current is achieved by MOSFET connected across the coils. The MOSFET is connected in a specific manner shown fig.1 & triggering of MOSFET by independent microcontroller bits in a specific pattern. The no. of MOSFET switch required for N coil is 2N+2. One MOSFET switch is connected to forward current & other to flow reverse current.

The speed is mainly depends on the switching delay of switches. So for a constant speed motor if torque is increased current also increase. So the current not exceed rated value a current sensing device is used. Current sensing device is connected to a serial ADC & ADC is communicated with microcontroller & switching delay is increased & speed is decreased correspondingly.

Forward switch on for a time period current flow in forward direction & than forward switch will off & reverse conduction switch will conduct then current flow in reverse direction in first coil & in a sequence reversal of current will take place in other coils. This switching pattern of the switches is continuing for next upcoming cycle.

II. SYSTEM DESCRIPTION

The main parts of electronic commutation dc machine

A. Stator

The stator core is made of insulated steel laminations. The thickness of the laminations and the type of steel are chosen to minimize eddy current and hysteresis losses. The magnetic path, which comprises a set of slotted steel laminations called stator core pressed into the cylindrical space inside the outer frame. The magnetic path is laminated to reduce eddy currents, reducing losses and heating. CRGO laminations of 0.5 mm thickness are used to reduce the iron losses. The stator frame is used to hold the armature windings. The coils are connected in series or parallel with MOSFET switch string for the forward & reverse conduction. The input is given at the terminals of the string at stator.

A.1 MOSFET required for Forward conduction & reverse conduction of coils

The N channel MOSFET are required for forward and reverse conduction of coils. So MOSFET should have less switching time. The rating of the MOSFET depends on peak voltage in coil. Triggering of MOSFET is using driver circuit with microcontroller bits in a specific manner.

For 24 slot 12 coils stator the connection diagram shown in fig.1 & physical installation is shown in fig.2. Gate pulse voltage is taken according to switching bit pattern. The no of MOSFET switch is 26.

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[1] Department of Electrical Engineering , BKBIET College, Pilani (Rajasthan), India, E-mail: rajendrabhamu045@gmail.com

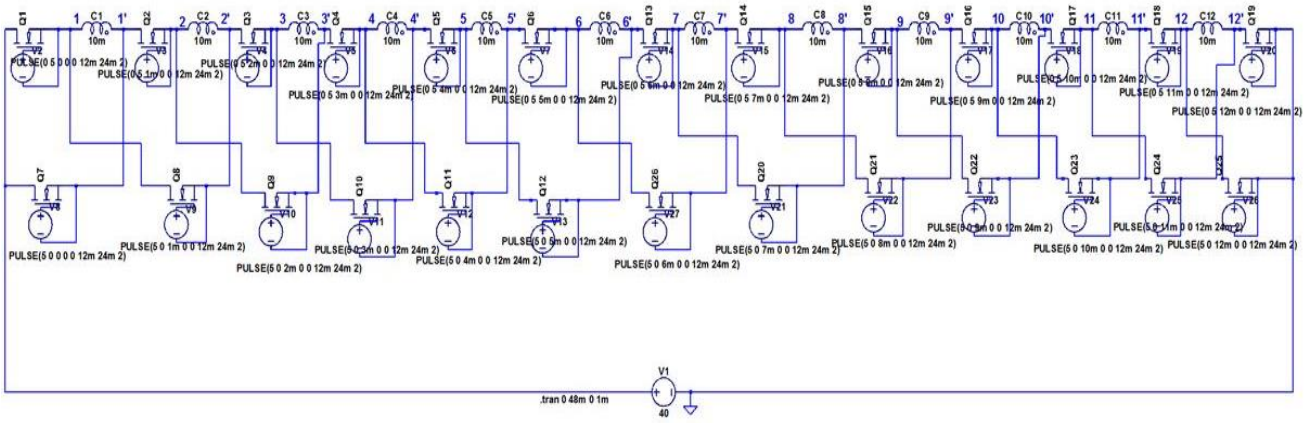

Fig.1: Coil connection with MOSFET switches for 2 pole motor.

A.2 Stator Winding (Armature Winding)

The coil side of coils are placed 180 electric degrees apart as shown in fig.2. One coil sides installed per slot. The connection of coils is in series with the MOSFET for forward and reverse conduction shown in fig.1. The coils are connected sequentially according the triggering sequence of MOSFET switch connected to coils. The positive and negative input terminals are given at two ends of coil connection. The connection shown in fig.1.

A.3 Microcontroller for MOSFET switch triggering

Microcontroller is required for specific triggering pattern of electronic MOSFET switch. Coding is done in KEIL & simulated in PROTEUS using microcontroller Atmel 89C51.

B. Rotor

The rotor may salient pole rotor or cylindrical rotor. Poles are built with thin silicon steel laminations of 0.5mm to 0.8 mm thickness to reduce eddy current.

In case of high speed the rotors are manufactured from solid steel forging. The rotor is slotted to accommodate the field winding. Normally two third of the rotor periphery is slotted to accommodate the winding and the remaining one third unslotted portion acts as the pole.

The rotor is excited by direct current supply with slip ring to create magnetic field flux [4].

B.1 Rotor Windings

In electronic commutation dc motor for rotor winding field poles is made of a number of coils circuit equal no of pole pairs is energized with dc power fed through slip ring riding on the shaft or may have permanent magnetic pole. The rotor winding can be wound separately, in series or parallel with armature winding.

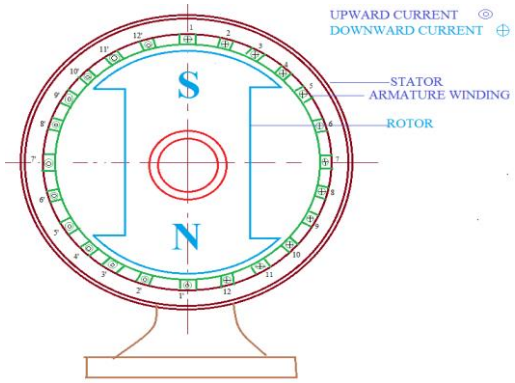

Fig.2: Physical installation of coil for a two pole motor.

III. WORKING PRINCIPLE:

The working principle of electronically commutation dc motor is using electronic MOSFET switch for commutation of the coils. Coils are installed in the stator slots. Coils are connected with MOSFET switches. Triggering of MOSFET switch is using microcontroller bits shown in fig 3. For a 12 coil 24 stator slots motor coils are connected with 26 MOSFET switches shown in fig1. Gate triggering pulse is given by microcontroller bits in a specific sequential manner. Using 26 independent bits of microcontroller port P_0, P_1, P_2 & two bit of P_3 simulated in KEIL & Proteus lab center electronics. The working of the motor is explained taking simple switches at place of MOSFETs.

Case 1: Switch status for switches shown in fig.4. So the direction of the flow of current in coils is known.. Coil C1 has no current & coils C2 to C12 having negative current. The physical installation of coils is shown in fig.5. The 24 slots are shown on the stator with black color indicate upward current, yellow color indicate downward current & blank indicate no current. So this will create two magnetic poles.

Case 2: Switch status for switches shown in fig.6. So Coil C1 has positive current & coils C2 has no current & coils C3 to C12 having negative current. So rotating armature magnetic field rotates one slot in anticlockwise direction as compare to case1. The physical installation of coils is shown in fig.7. So the stator poles shifts one slot in clockwise direction & rotor will follow this.

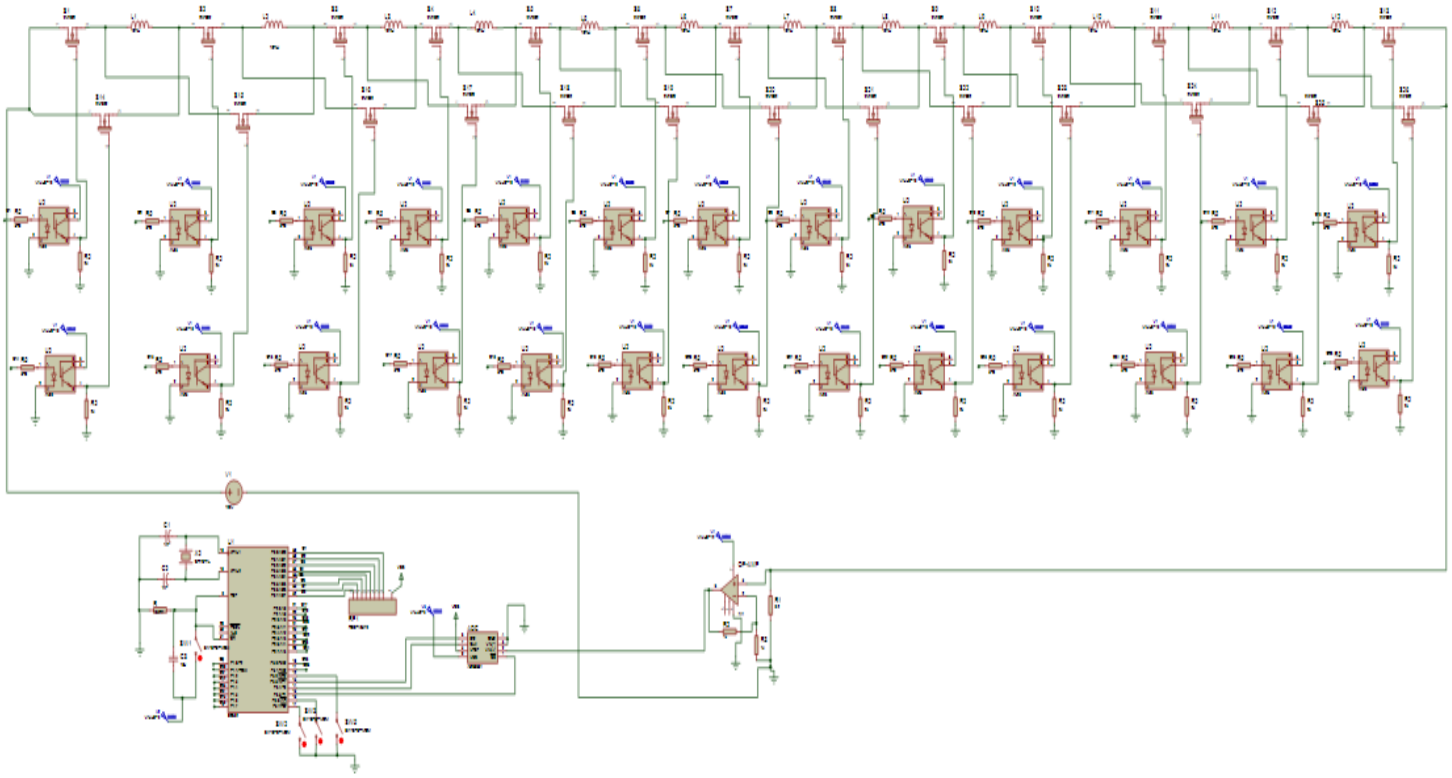

Fig.3: Circuit diagram for stator (armature) coil commutation & current sensing circuit with A–D converter.

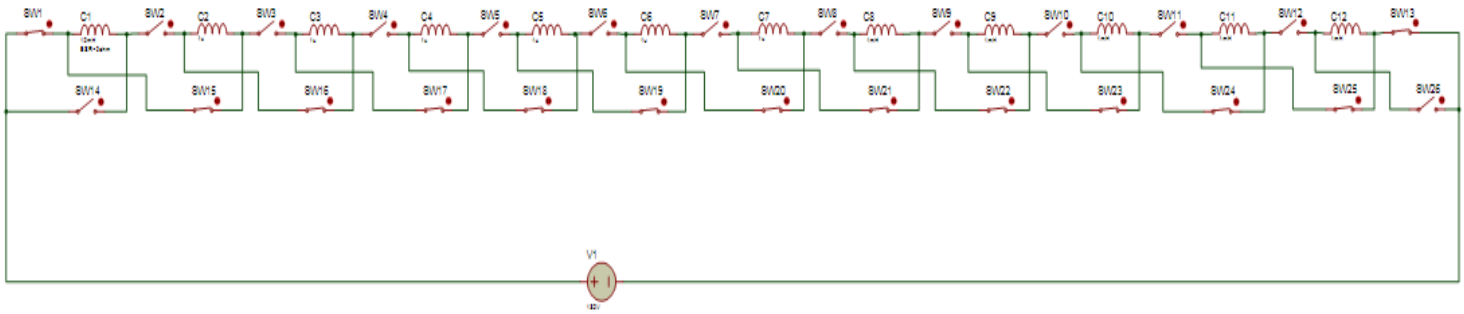

Fig.4: Circuit diagram for switch status & stator (armature) coil current flow direction for case1.

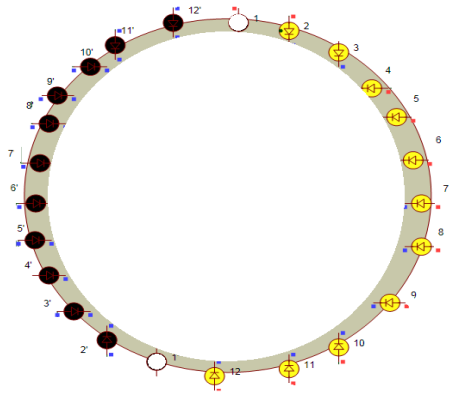

Fig.5: Physical coil installation & stator (armature) coil current flow direction for case1.

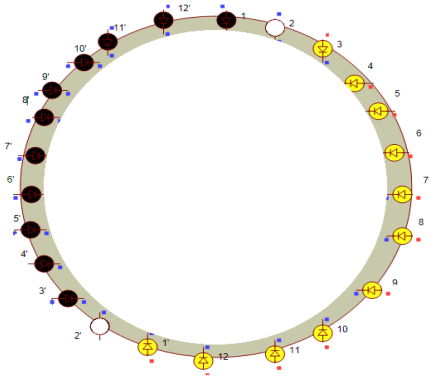

Fig.7: Physical coil installation & stator (armature) coil current flow direction for case2.

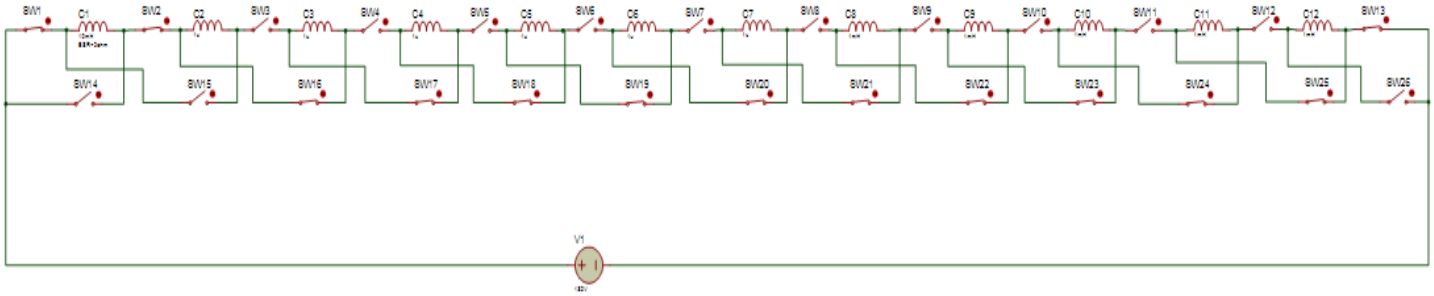

Fig.6: Circuit diagram for switch status & stator (armature) coil current flow direction for case2.

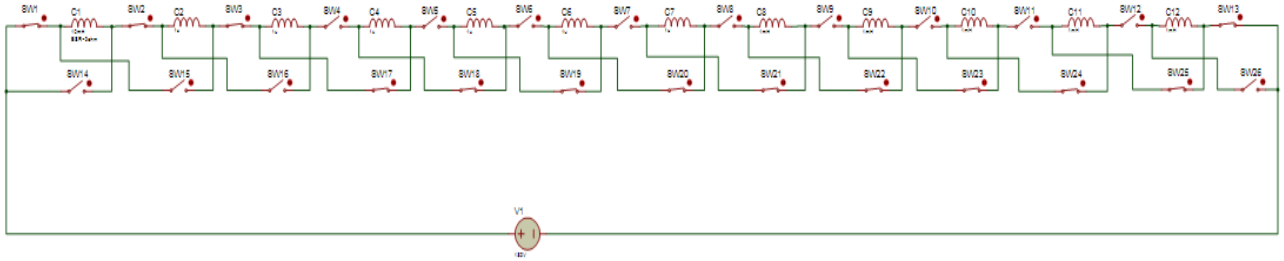

Fig.8: Circuit diagram for switch status & stator (armature) coil current flow direction for case

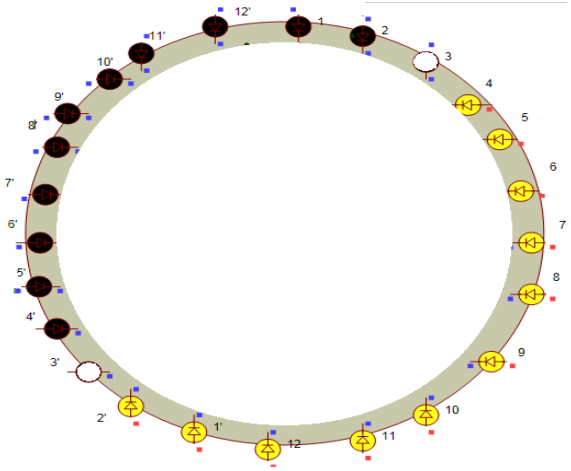

Fig.9: Physical coil installation & stator (armature) coil current flow direction for case

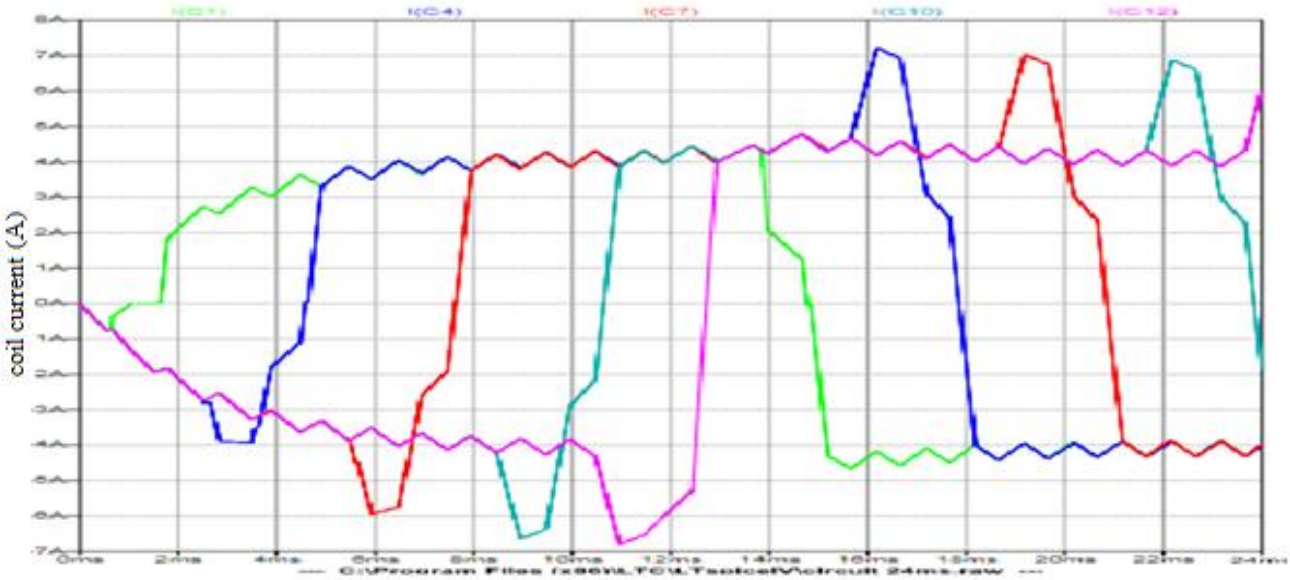

Fig.10: Current waveform in various coils C1, C4, C7, C10, and C12.

Case 3: Switch status for switches shown in fig.8. So Coil C1, C2 have positive current & coils C3 has no current & coils C4 to C12 having negative current. The physical installation of coils is shown in fig.9. So the stator poles again shifts one slot in clockwise direction & rotor will follow this.

So this sequence will be continue in upcoming cases & Case 4 to case 26 the rotor will complete one cycle & this will repeats in next cycles.

Before reversal current will zero for little time in each coil. So, current reversal of coil is reliable.

Simulation of the circuit diagram using triggering pattern of switches given above is performed in LT SPICE & PROTEUS LABCENTER ELECTRONICS software for simultaneous waveform in one figure. A Wave form of current flow is shown in fig.10 for one cycle & it repeats for next upcoming cycles. Current in coil 1 is positive for first half cycle & negative for next half cycle. Current in coil 2 lag by current in coil 1. Current in coil 2 is negative for starting time than positive for half time and again current be negative.

So the flow of current in next coil lag previous coil. Current in all coils is negative for half time period & positive for half time period. By changing direction of current flow in coils sequentially the magnetic field changes. Magnetic field is rotating in nature & field poles rotate with magnetic field. The time delay in two consequent triggering can be adjusted constant, increasing, decreasing & exponential increasing or decreasing. So speed of the motor can be obtained in desired way so motor have a flexible speed characteristic. The motor rotation can be easily reversed by microcontroller pin P3_7.

For proper visualization current waveform for coils C1, C4, C7, C10 and C12 are shown in fig.10. The value of supply voltage is taken $V_s = 180V$. Coil inductance is taken $L = 10\text{m}$ hennery with series resistance of $R_a = 2\Omega$.

Time cycle is $t = 24\text{ms}$. Then the speed of rotation approximates $W_m = 41.6$ rps & $2500\ rpm$. So for any time 11 coils will conduct with 13 MOSFET switches. KVL equation

(I_a = *Average armature current, A; P =no. of poles. i =Peak - peak armature current, A; Z =no. of conductors*

V_{sw} =MOSFET on state drop, A =no of parallel path T =Motor output torque, Nm; ϕ =flux per pole, Wb)

$$V_s = 11 * E_b + (11 * I_a * R_a) + 13 * V_{sw} \quad (1)$$

The back emf in each coil is

$$E_b = \frac{Li}{t} * \frac{2}{p} = \left(\frac{P*Z*\phi}{A} * n = \frac{Li}{t} * \frac{2}{p}\right)$$
$$= 10m * \frac{14}{24m} = \frac{70}{12} = 5.833V \quad (2)$$

So emf in all 11 coils connected in series is 64.16V.
Voltage drop in resistance

$$I_a * R_a = 4.5 * 2 = 9V \quad (3)$$
$$V_{sw} = 1.294\text{V} \quad (4)$$

Output torque for the motor

$$T = (E_b * I_a) / W_m = \frac{64.16*4.5}{2\pi*41.6} = 1.1047\text{Nm} \quad (5)$$

So for a rated constant power motor if torque is increase above a limit than speed should decrease. So in this type

IV. Starting & Speed Control

At starting due to rotor inertia the switching speed of the coils should be low. So reduce voltage should be applied. So with the reduced voltage the switching time should be high to rotor gain sufficient speed.

1. At reduced voltage microcontroller pin P3_2=0 for little time. Then the switching time of coils will be high & rotating speed will low so rotor can easily rotate with field. After few cycles pin P3_6=0 for little time to increase speed. Then applied voltage is increased to rated value.

2. The speed is regulated by switching delay of the coils. To increase the speed microcontroller pin P3_6=0 for little time & decrease the speed microcontroller pin P3_2=0 for little time. So speed can be regulated on desired speed from minimum to maximum speed.

V. Regenerative Breaking

Regenerative braking is used at time of speed decreasing or stopping. So at this time pin P3_6 =0 make high & field excitation is increased. All switches have high gate signal so behaves like diodes. The kinetic energy of rotor can used to generate electric power & the electric power is feedback to supply source.

Motor speed can be easily controlled as torque depends on speed. So the current sensing device is used to decrease speed if current is increasing above a limit.

VI. Conclusion

In electronic commutation motor the working is similar to DC motor & the mechanical commutation using brush is replaced by connecting MOSFET switch. More features can be added through coding. The switching pattern for triggering can be programmed in desire way for a microcontroller. The speed can be obtained constant, discrete, linearly increasing & decreasing & exponential increasing or decreasing or any type of curvature nature. So speed of the motor can be obtained in desired way so motor have a flexible speed characteristic. There is no commutation problem & maintenance problem. Microcontroller & MOSFET switch required.

- No commutation & maintenance problem.
- Flexible speed characteristic.

- Winding configuration for no. of parallel path to adjust source V - I rating.
- Starting & speed control easy as motor can run on any desired speed.
- Highly reliable & efficient motor.
- Regenerative braking is possible.

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BIOGRAPHY

Rajendra Bhamu was born in Sujangarh, Rajasthan, India in 1993. He is pursuing his B.Tech degree in Electrical Engineering from BKBIET College, Pilani (Rajasthan), India. His interest to study for higher education at premier and reputed institute. And his research interests focus on reliable & efficient power system through electronics & automation and utilize renewable energy sources.

Design Optimization for Low Voltage DC-DC Converter with Coupled Inductor Topology

Basavaraj V. Madiggond [1] H. N. Nagaraja [2]

Abstract–Multiphase Synchronous Buck Converters also known as voltage regulator modules (VRMs) for microprocessor power delivery with coupled inductors at output are discussed. For feasible and effective ripple reduction, strong coupling is needed if the correct magnetic topology is used. For more than two phases, this can be a "ladder" core with windings around each rung. Typical ripple reduction is better than a factor of six with no effect on response time. One can also chose to improve response time while still significantly reducing ripple.

Key Words–Synchronous Buck Converter, Multiphase, Transient response, Coupled Inductor, Coupling coefficient.

I. INTRODUCTION

It is predicted that the future microprocessors demand more and more power and at the same time the required voltage levels continue to drop. In future voltage go below 1V and current will go beyond 100A [1]. To handle this huge current multiphase interleaving technology is preferred. The multiphase interleaving technology helps to reduce the current ripples at the output and improves the transient response [2]-[4]. The challenge is that the load current can change from near zero to full load or vice versa in nanoseconds and the voltage has to be maintained constant throughout. The combination of high current and fast response requires a voltage regulator module (VRM) located immediately adjacent to the load. The VRM must be small in size as well as have high efficiency and extremely fast response.

At present, the standard design used for high-performance VRMs is a buck converter with multiple parallel sections, staggered in phase [5], [6], In a buck converter with a load-current step, the output capacitor supplies (or sinks) the immediate difference in current while the inductor current is ramped up or down to match the new load current. A small inductor allows ramping the current quickly to minimize the output capacitor requirement. However, small inductor values also lead to large ripple current. In a single-phase converter, large ripple current in the inductor increases the output capacitor requirement when the inductor is very small [6]. The standard multiphase interleaved design avoids this problem because it achieves substantial ripple current cancellationin the output capacitor [7]. This allows smaller inductance without requiring a large output capacitor. However, the full ripple current flows through the MOSFET switches (including synchronous rectifiers) and through the inductor itself, resulting in higher losses and higher peak current requirements. One strategy to reduce the ripple current throughout is to operate at very high switching frequencies (e.g., see [6]), but this increases switching and gate-drive losses and imposes difficult requirements for magnetic materials capable of low loss at very high frequencies.

In [8], [9], it was shown that coupling the inductors in a two-phase interleaved converter can effect a reduction in ripple. Unlike the ripple cancellation in an uncoupled multiphase converter, this ripple reduction extends to the current in the inductor windings and in the switches. In [10], one topology for coupling larger numbers of inductors in a multiphase VRM is considered, but is not found to offer major advantages. In [11], design optimization of the coupled inductor is considered. However, the method employed there does not provide any insight regarding the influence of the design parameters on the losses and the performance of the converter.

In this paper, a novel coupled core structure along with a new method for estimating the losses and efficiency is proposed. The proposed core structure is shown in Fig. 1. It has a central leg called the leakage leg, surrounded by '*n*' number of side legs. The central leg has an adjustable air gap. By adjusting the length of the air gap the coupling coefficient can be varied. As the central leg is equidistant from the surrounding legs, the reluctance offered to individual phase flux are identical.

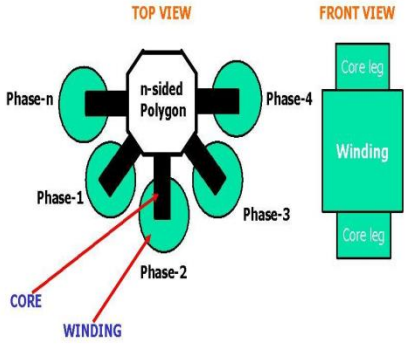

Fig. 1: Proposed coupled multiphase buck converter structure

II. ANALYSIS OF THE UNCOUPLED INDUCTOR BUCK CONVERTER

There are three main limitations of the single-phase buck regulator if employed in a voltage regulator for desktop, notebook or server applications. First, the high currents — greater than 40 A for notebook, 120 A for desktop and 150 A for server — would cause excessive I^2R losses if delivered over one path or phase. Second, processors require low-output ripple voltage and this necessitates keeping the output ripple current low, as $V_{RIPPLE} = I_{RIPPLE}$ ESR. This implies the need for a large inductor because I_{RIPPLE} is proportional to 1/L.

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[1] **Jain College of Engineering, Belgaum, Karnataka, India, E-mail: basavarajvma@gmail.com**
[2] **Dean (Academics), Indus University Ahmedabad, Gujarat, India**

Third, the processor power supply must be able to respond quickly to changes in power requirements. Unfortunately, the third requirement, fast transient response, implies the need for a small inductor to allow the current through the supply to change quickly, and this conflicts directly with the need for a larger inductor to minimize output voltage ripple.

The uncoupled multiphase buck regulator was designed to resolve these three limitations. Instead of using a single high-current path, the multiphase buck breaks the current into several lower current parallel paths or phases. Each phase has its own inductor and set of switches, and the current in each phase is summed to form the output current. By activating each phase at a different point in the cycle, the ripple currents of each phase can be overlapped to reduce the overall output current ripple. To simplify the analysis, a two-phase uncoupled buck with 180 degrees between phases will be discussed here. However, the same approach can be used with any number of phases operating at any phase angle.

A simplified schematic of a two-phase buck is shown in Fig. 2. A two-phase buck has four states of operation. During the first state, the input voltage is connected to phase one, and energy is both being transferred to the output and stored in the inductor L1. At the same time, the input side of phase two is connected to ground and the inductor L2 transfers energy to the output. During the second state, the input sides of both phases are connected to ground and both inductors (L1 and L2) transfer energy to the output. This cycle is repeated over states three and four, the only difference being that phase two is connected to the input while phase one is connected to ground, and then both phases are connected to ground.

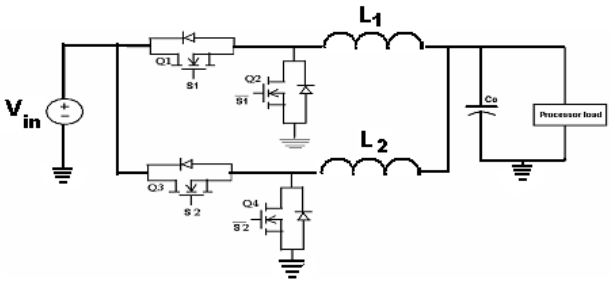

Fig. 2: Uncoupled Two phase synchronous buck converter

III. Analysis of the Coupled Inductor Buck Converter

In the proposed core structure, any number of phases can be coupled. Fig. 3(a) shows the general schematic diagram of an *n* phase coupled buck converter. Under the assumptions of identical phases and ideal switches, the equivalent representation of an *n* phase coupled buck converter is shown in Fig. 3(b).

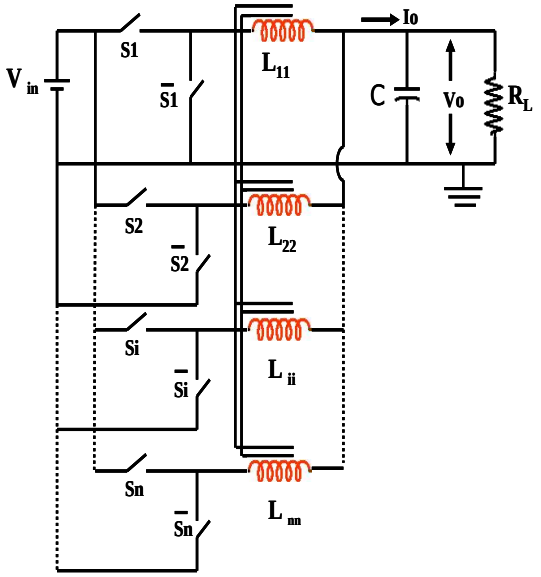

Fig. 3(a): General schematic diagram of an n phase coupled buck converter

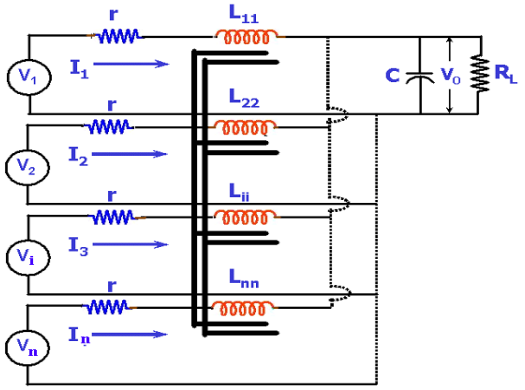

Fig. 3 (b): Coupled multiphase buck converter with filter inductor in each phase

where,

$$V_i = V_{in}.S_i \qquad (1)$$

$$S_i = 1 \; ; \quad for \; \frac{(i-1)}{n}.T \le t \le \frac{(i-1)}{n}.T + T_{on}$$
$$= 0;$$

Otherwise

$$T_{on} = D.T$$

where,
'*D*' is the duty cycle; *T* is the switching period; and '*n'* is the number of phases. It was shown in [12] that, such a coupled buck converter can be represented by one common mode and (*n-1*) differential mode equivalent circuits provided the self and mutual inductances of all the phases are identical. These equivalent circuits are shown in Fig. 4(a) and 4(b).

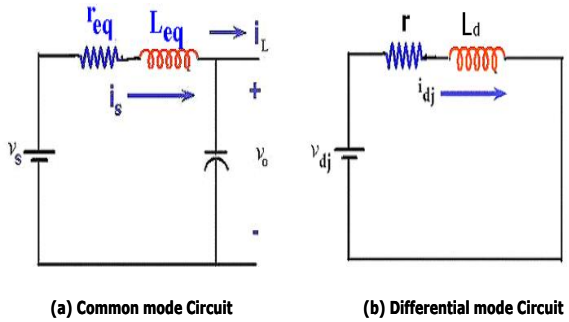

Fig. 4. Coupled converter equivalent circuits

where,

$V_s \triangleq \frac{1}{n}\sum_{i=1}^{n} Vi$; $i_s \triangleq \sum_{i=1}^{n} ii$; $r_{eq} \triangleq \frac{r}{n}$

$$Leq \triangleq \frac{Ls}{n} = \frac{L - \sum_{i=1}^{n-1} Mi}{n}$$

For $2 \le j \le n$

$V_{dj} \triangleq V_{j-1} - V_j = r i_{dj} + L_d \, p \, i_{dj}$;

$I_{dj} \triangleq i_{j-1} - i_j$;

$L_d = (L+M) \, . \, I_{(n-1).(n-1)}$

IV. COUPLED CORE DESIGN OF MULTIPHASE BUCK CONVERTER

The coupled inductor concept and its advantages may be extended to any number of phases. For simplicity, we have taken a four-phase coupled structure, maintaining the shape of the core to be the same. The four coils are connected in the four legs of the new core structure. It should be noted that, due to the structural symmetry of the proposed core, the assumptions made for deriving the common mode and differential mode equivalent circuits will be satisfied.

During the steady state, a part of the flux produced by the inductor currents passes through the center leg. The center leg has an air gap, whose length can be adjusted for achieving a better coupling coefficient. Higher the coupling, greater is the ripple reduction. Even the transient response has found to be improved by experiment. In the phase legs, the flux produced by one coil opposes the other. In the new proposed core structure, our intention is to draw less Ampere turn from the source and meet the requirement. Here, the intention is to avoid saturation of the core and as far as possible use all the windings equally. Fig. 5 shows the electrical equivalent model of the multiphase coupled core structure shown in Fig. 1.

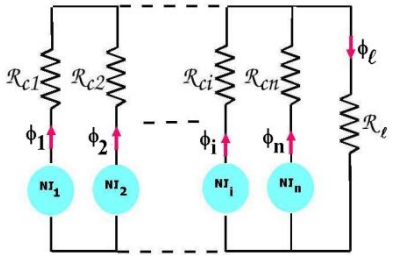

Fig.5. Electrical Equivalent model for multiphase coupled core structure R c and Rl are the core and leakage path reluctance respectively.

The equivalent reluctance as seen by each MMF source of the model shown in Fig. 5 is

$$\mathcal{R}_{eq} = \mathcal{R}_c + \frac{\frac{\mathcal{R}_c}{n-1}.\mathcal{R}_f}{\frac{\mathcal{R}_c}{n-1} + \mathcal{R}_f} \qquad (2)$$

Where, $\mathcal{R}_c$ is the reluctance of each core leg and $\mathcal{R}_f$ is the reluctance of the central leakage path.

$$\therefore \mathcal{R}_{eq} = \mathcal{R}_c \cdot \frac{1 + n.k_r}{1 + (n-1).k_r} \quad ;$$

$$\text{where } k_r = \frac{\mathcal{R}_f}{\mathcal{R}_c} \qquad (3)$$

The self and mutual inductances of the coupled inductor are

$$L = \frac{N_c^2}{\mathcal{R}_{eq}} = \frac{N_c^2}{\mathcal{R}_c} \frac{1 + (n-1).k_r}{1 + n.k_r} \quad ; \qquad (4)$$

n = number of phases; N_c is the number of turns in each phase leg

$$M = \frac{N_c^2}{\mathcal{R}_c} \times \frac{k_r}{1 + n.k_r} \qquad (5)$$

The common mode and the differential mode inductances are given by

$$L_{eq} \triangleq \frac{Ls}{n} = \frac{L-(n-1)M}{n} = \frac{Nc2}{nRc} \cdot \frac{1}{1+nkr}$$

$$L_d = L + M = \frac{N_c^2}{\mathcal{R}_c} \qquad (6)$$

Using the model shown in Fig. 5, we intend to calculate the magnetic flux waveform which has both dc and ac components. The dc components are calculated by assuming that the dc currents in each phase are equal. Thus, for 'n' phases connected in parallel, the dc component of phase current is given by $\frac{I_S}{n}$.

Flux in the core phase legs:

With reference to the Fig. 5, flux in each phase leg is given by

$$\phi_i = \phi_{ii} - \sum_{\substack{j=1 \\ i \neq j}}^{n} \phi_{Mj} \tag{7}$$

where, ϕ_{ii} is the total flux produced in the leg i, ϕ_{Mj} is the mutual flux due to the j^{th} coil.

$$\phi_i = \frac{1}{N_C}\left[L.i_i - M\sum_{\substack{j=1 \\ j \neq i}}^{n} ij \right] = \frac{1}{N_C}\left[(L+M).i_i - M.i_S \right] \tag{8}$$

$$\phi_i = \frac{N_c}{\mathcal{R}_c}[i_i - \frac{k_r}{1+n\cdot k_r}\cdot i_S] \tag{9}$$

$\therefore$ Peak value of

$$\phi_i = \phi_i = L_d.\hat{I}_{pc} - M.\hat{I}_s$$

Now,

$$\frac{\Delta I_{pc}}{I_{pc}} = \left[1 + \frac{(n-1)}{(1-n.D)}.\frac{L_s}{L_d}\right].\frac{\Delta I_s}{I_s}$$

$$\therefore \hat{\phi}_i = \frac{N_c I_s}{\mathcal{R}_c}[\frac{(1-n\cdot D)+\frac{1}{2}.n.(1-D)\frac{\Delta I_s}{I_s}}{n.(1+n\cdot k_r)(1-n\cdot D)}]$$

Peak flux density in the core legs is given by

$$\hat{B}_i = \frac{\hat{\phi}_i}{A_c} \tag{10}$$

where, A_c is the phase leg cross sectional area Flux in the leakage path (central leg)

From Fig. 5

$$\phi_l = \frac{\frac{\mathcal{R}_c}{(n-1)}}{\frac{\mathcal{R}_c}{(n-1)} + \mathcal{R}_l}.\sum_{i=1}^{j}\phi_{ii} \tag{11}$$

$$OR \quad \phi_l = \frac{\mathcal{R}_c}{\mathcal{R}_c + (n-1).\mathcal{R}_l}\cdot\frac{N_c\cdot I_s}{\mathcal{R}_{eq}}$$

$\therefore$ Peak value of ϕ_l is given by

$$\hat{\phi}_l = \frac{N_c I_s}{(1+n.k_r)\cdot\mathcal{R}_c}[\frac{1}{n} + \frac{1-D}{1-n.D}\cdot\frac{1}{2}\cdot\frac{\Delta I_s}{I_s}] \tag{12}$$

$\therefore$ Peak flux density in the leakage path is

$$\hat{B}_l = \frac{\hat{\phi}_l}{A_l} \tag{13}$$

where A_l is the central leg cross sectional area Ac flux in the core legs

$$\Delta\phi_i = \frac{(1-D).N_c\cdot\Delta I_s}{(1-n.D).(1+n.\ k_r)\cdot\mathcal{R}_c} \tag{14}$$

$$\Delta B_i = \frac{\Delta\phi_i}{A_c} \tag{15}$$

Ac flux in the leakage path

$$\Delta\phi_l = \frac{N_c\cdot\Delta I_s}{(1+n.\ k_r)\cdot\mathcal{R}_c} \tag{16}$$

$$\Delta B_l = \frac{\Delta\phi_l}{A_l} \tag{17}$$

1). Loss estimation in the Coupled Converter

Fig. 6 shows the cross sectional diagram of coupled core structure

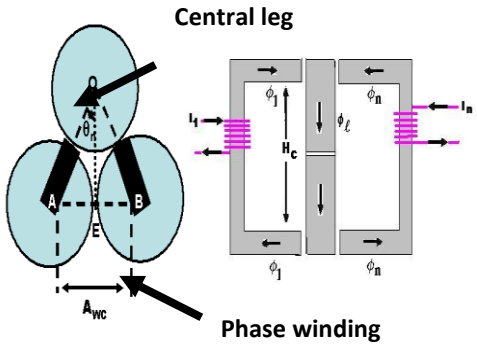

Fig. 6. Cross sectional view of the coupled core structure

With reference to Fig. 6,

$\frac{A_{WC}}{2}$ =Window area,

A_c =Core area, H_c =Window height

Volume of outer legs:

Length of each outer leg =

$$(H_c + \sqrt{A_c}) + 2.[\frac{A_{wc} + \sqrt{A_c}.H_c}{2.H_c.\sin\theta_n} - \sqrt{\frac{A_l}{\pi}}] \tag{18}$$

Total volume of the core with '*n*' legs

$$= \frac{n.A_c.H_c}{\sin\theta_n}.[\sin\theta_n + \frac{\sqrt{A_c}}{H_c}.\left\{1 + \sin\theta_n(1 - \frac{2}{\sqrt{\pi}}\sqrt{\frac{A_l}{A_C}}\right\} + \frac{A_{WC}}{H_c^2}] \tag{19}$$

Assuming the core loss to be W_i / unit volume at $\Delta B = B_{max}$ and $f = f_{sw}$

Core loss in the outer phase legs is= $W_i\cdot(\frac{\Delta B_i}{B_{max}})^2$ * Total volume of phase legs

$$= W_i\cdot\left(\frac{\Delta I_s.N_c}{A_c.\mathcal{R}_c.B_{max}}\right)^2\cdot\frac{(1-D)^2}{(1-n.D)^2.(1+n.k_r)^2}$$

$$*[\frac{n.A_c.H_c}{\sin\theta_n}\left\{\sin\theta_n + \frac{\sqrt{A_c}}{H_c}(1+\sin\theta_n - \frac{2}{\sqrt{\pi}}.\sqrt{\frac{A_l}{A_c}}.\sin\theta_n) + \frac{A_{WC}}{H_c^2}\right\} \tag{20}$$

Volume of leakage path

$$= (H_c + \sqrt{A_c}).A_l \quad (21)$$

Core loss in leakage path = $n.W_i.(\frac{\Delta B_l}{B_{max}})^2$ *

Volume of the leakage path =

$$W_i.\left(\frac{\Delta I_s.N_c}{A_c.\mathcal{R}_c.B_{max}}\right)^2.\frac{n}{(1+n.k_r)^2}.\left(\frac{A_c}{A_l}\right)^2.[H_c.A_c(1+\frac{\sqrt{A_c}}{H_c}).\frac{A_l}{A_c}] \quad (22)$$

Therefore total losses in the coupled core can be expressed as

$$W_{ic} = n.W_i.H_c.A_c.\left(\frac{\Delta I_s.N_c}{A_c.\mathcal{R}_c.B_{max}}\right)^2.\frac{1}{(1+n.k_r)^2}[\frac{(1-D)^2}{(1-n.D)^2.\sin\theta_n} * \left\{\sin\theta_n + \frac{\sqrt{A_c}}{H_c}(1+\sin\theta_n - \frac{2}{\sqrt{\pi}}.\sqrt{\frac{A_l}{A_c}}.\sin\theta_n) + \frac{A_{wc}}{H_c^2}\right\} + .(1+\frac{\sqrt{A_c}}{H_c}).\frac{A_c}{A_l}] \quad (23)$$

Losses in the MOSFETS:

Assuming the $R_{DS\text{-}ON}$ of the high side and low side MOSFETS to be the same, the losses during steady state is given by,

$$W_{MOSFET} = n * I_{RMS}^2 * R_{DS\text{-}ON};$$

where, $I_{RMS} = \frac{I_s}{n} * (1 + \frac{K_C^2}{12})^{\frac{1}{2}}$

$$W_{MOSFET} = \frac{I_s^2}{n} * (1 + \frac{K_C^2}{12}).R_{DS-ON} \quad (24)$$

where, $K_C = \left[\frac{n*[(1-D)+K*(1-n.D)]}{(1-n.D)*(1+n.K)}\right].\frac{\Delta I_s}{I_s}$

$K = \frac{M}{L} = \frac{k_r}{1+(n-1).k_r}$ = Coupling coefficient;

D = Duty ratio

Loss in the Inductor due to ESR:

$W_{L\,(ESR)} = I^2_{RMS} * ESR_L$

ESR_L is given by $[\frac{\pi.\rho.N_c^2}{H_c} + \frac{\pi.\rho.N_c.\sqrt{A_c}}{C_w}]$

where ρ is the specific resistance of the winding material, C_w is the winding cross sectional area.

$$W_{L(ESR)} = \frac{I_s^2}{n^2} * (1 + \frac{K_C^2}{12}) [\frac{\pi.\rho.N_c^2}{H_c} + \frac{\pi.\rho.N_c.\sqrt{A_c}}{C_w}] \quad (25)$$

Therefore, total loss in the coupled core topology is given by,

$W_{total} = W_{ic} + W_{MOSFET} + W_{L\,(ESR)}$

$$W_{total} = n.W_i.H_c.A_c.\left(\frac{\Delta I_0.N_c}{A_c.\mathcal{R}_c.B_{max}}\right)^2.\frac{1}{(1+k_r)^2}[\frac{(1-D)^2}{(1-n.D)^2.\sin\theta_n} * \left\{\sin\theta_n + \frac{\sqrt{A_c}}{H_c} * (1+\sin\theta_n - \frac{2}{\sqrt{\pi}}.\sqrt{\frac{A_l}{A_c}}.\sin\theta_n) + \frac{A_{wc}}{H_c^2}\right\} + (1+\frac{\sqrt{A_c}}{H_c}).\frac{A_c}{A_l}] + \frac{I_0^2}{n}(1+\frac{K_c^2}{12}) * [R_{DS-ON} + \{\frac{\pi.\rho.N_c^2}{H_c} + \frac{\pi.\rho.N_c.\sqrt{A_c}}{C_w}\}] \quad (26)$$

2). Loss estimation in uncoupled case

Fig. 7 shows the cross sectional view of the uncoupled core structure.

The maximum ac flux flowing in the core is given by

$$\hat{\phi}_{max} = \frac{N_u.I_s}{\mathcal{R}_u}[\frac{1}{n} + \frac{\Delta I_s}{2.I_s}.\frac{(1-D)}{(1-n.D)}] \quad (27)$$

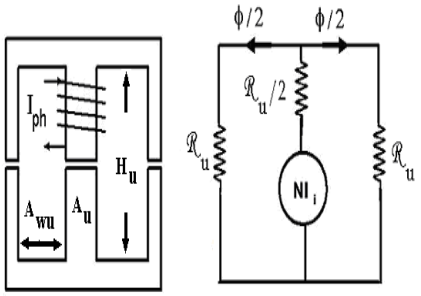

Fig. 7: Uncoupled core structure with its equivalent model

where, I_O is the output load current, D is the duty cycle and N_u is the number of turns in the winding.

Ac flux in the core, is given by

$$\Delta\phi_i = \frac{N_u.\Delta I_O}{\mathcal{R}_u}\frac{(1-D)}{(1-n.D)} \quad (28)$$

Total core loss in the uncoupled core is given by

$$W_{iu} = W_i.\left(\frac{\frac{\Delta\phi_t}{A_u}}{\frac{\hat{\phi}_{Max}}{A_u}}\right)^2 * \text{Volume of the core}$$

A_u is the core cross sectional area, $\mathcal{R}_u$ is the reluctance of the core leg

$$W_{iu} = W_i.\left(\frac{N_u.\Delta I_0}{A_u.\mathcal{R}_u.B_{max}}\right)^2.\frac{(1-D)^2}{(1-n.D)^2}.[n.\frac{A_u}{H_u}(2.H_u^2 + 2.A_{wu} + 2.H_u.\sqrt{A_u})] \quad (29)$$

Loss in the Inductor due to ESR:

$W_{L\,(ESR)} = I^2_{RMS} * ESR_L$

$$W_{L(ESR)} = \frac{I_O^2}{n^2} * (1 + \frac{K_U^2}{12}) \left[\frac{\pi.\rho.N_U^2}{H_U} + \frac{\pi.\rho.N_U.\sqrt{A_U}}{C_w}\right] \quad (30)$$

where, $K_U = \frac{n.(1-D)}{(1-n.D)}$

Loss in the MOSFET due to $R_{DS\text{-}ON}$

$$W_{MOSFET} = \frac{I_O^2}{n} * (1 + \frac{K_U^2}{12}).R_{DS-ON} \quad (31)$$

$\therefore$ Total loss in the uncoupled circuit is

$$W_{u\text{-}total} = n.W_i.H_u.A_u.\left(\frac{N_u.\Delta I_0}{A_u.\mathcal{R}_u.B_{max}}\right)^2.\frac{(1-D)^2}{(1-n.D)^2}.(2+2.\frac{A_{wu}}{H_u^2}+2.\frac{\sqrt{A_u}}{H_u}) + \frac{I_0^2}{n.(1-D)}(1-D+2.K_u.D-2.D^2.K_u+D^2.K_u^2-\frac{D}{12}.K_u^2+\frac{K_u^2}{12})* (\pi.\rho.\frac{N_u^2}{H_u}+\pi.\rho.\frac{N_u.\sqrt{A_u}}{C_w}+R_{DS\text{-}ON}) \quad (32)$$

LOSS FUNCTION = *Ratio of coupled to uncoupled total losses* (Eqn. 26 and 32)

$\therefore$ LOSS FUNCTION

$$= \frac{W_{ic} + W_{L(ESR)} + W_{MOSFET}}{W_{iu} + W_{L(ESR)} + W_{MOSFET}}$$

After taking the ratio of total losses between coupled and uncoupled converters, we have further expressed the coupled terms in terms of uncoupled parameters, so as to get all unknown coupled variables in terms of known uncoupled variables with valid assumptions.

V. Optimization of Loss Function

In order to estimate the efficiency improvement and to predict the losses in the coupled system, a comparative analysis between uncoupled and coupled is made by taking the ratios of many variable parameters viz.,

$X = \frac{A_{wu}}{A_u}$ = Ratio of window to core area in uncoupled case equal to 1.5 (assumed)

$X1 = \frac{A_c}{A_u}$ = Ratio of coupled to uncoupled core cross sectional areas

$X2 = \frac{N_c}{N_u}$ = Ratio of coupled to uncoupled number of turns.

$X3 = \frac{A_{wc}}{A_c}$ = Ratio of window to core cross sectional area in the coupled converter

$X4 = \frac{l_l}{l_c}$ = Ratio of leakage air gap length to core air gap length in coupled core

$X5 = \frac{A_c}{A_l}$ = Ratio of core to leakage path cross sectional area in coupled converter

$X6 = \frac{H_c}{H_u}$ =1 (assumed)

The basis of comparison are $I_s=I_o$, $L_s = \frac{L_u}{n}$; where L_u is the self-inductance of the coil L_s is the equivalent inductance

1). Constraint equations:

The loss function to be optimized has the numerator and denominator terms in the six variables mentioned above. We have used Lagrange's method of optimization. The constraint equations we have considered are as follows:

a) Equality constraint equations:-

- *Foot print area ratio is equal to 1*

$$1.046 * X_1^2 * X_3^2 + 4.58 * X_1 + 4.71 * X_2^2 + 4.37 * X_1^{\frac{3}{2}} * X_3 + 9.28 * X_1^{\frac{1}{2}} * X_2 + 4.435 * X_1 * X_2 * X_3 - 61.4 = 0$$

- *Equivalent coupled inductance is 1/n times the equivalent uncoupled inductance.*

$$X_1 * X_2^2 - 4 * X_4 * X_5 - 1 = 0$$

b) Inequality constraint equations:-

- *Window area per turn in coupled case is greater than or equal to that of uncoupled case*

$$X_1.X_3 - 3.X_2 \geq 0$$

- *The weight of the coupled system must be less than or equal to the weight of the Uncoupled system*

$$24 * X_1 + 47.33 * X_1^{\frac{3}{2}} - 44.35 * X_1^{\frac{3}{2}} / sqrt(2 * X_1 * X_2^2 - 1) + 22.64 * X_1^2 * X_3 + 23.77 * X_1 / (2 * X_1 * X_2^2 - 1) + 19.4 * X_1^{\frac{3}{2}} / (2 * X_1 * X_2^2 - 1) + 56.08 * X_1^{\frac{3}{2}} + 22.9 * X_1^2 * X_3^2 \leq 509.72$$

- *Leakage leg area must be less than or equal to the difference of foot print area and the sum of core and winding area.*

$$\frac{4}{2.X_1.X_2^2 - 1} - 1.04 * X_1.X_3^2 + 14.14.\frac{X_2^2}{X_1} - 4.37 * \sqrt{X_1}.X_3 + 21.5.\frac{X_2}{\sqrt{X_1}} - 4.44.X_2.X_3 + 8 \leq 0$$

Table 1:Loss estimation in coupled core with variation of foot print area ratio

Variables	FPA ratio at weight ratio=1									
	0.6	**0.7**	**0.8**	**0.9**	**1.0**	**1.1**	**1.2**	**1.3**	**1.4**	**1.5**
X_1	2.51	3.037	3.19	3.335	3.47	3.6	3.73	3.85	3.96	4.07
X_2	0.51	0.465	0.45	0.434	0.42	0.41	0.40	0.395	0.388	0.38
X_3	0.61	0.586	0.68	0.758	0.83	0.88	0.94	0.987	1.03	1.07
Loss ratio	0.91	0.907	0.905	0.902	0.9	0.899	0.898	0.897	0.896	0.89

$$X_1 = \frac{A_C}{A_U};\ X_2 = \frac{N_2}{N_1};\ X_3 = \frac{A_{WC}}{A_C};\ X_4 = \frac{l_l}{l_g} = 1;\ X_5 = \frac{X_1 X_2^2 - 1}{4};\ X_6 = 1;$$

The coupled loss ratio obtained by the optimization of the loss function for different foot print area ratio is as shown in Table 1. The loss ratio between coupled to uncoupled converter circuits, is decreasing with the variation of foot print area (FPA) ratio. The maximum ratio is 91% at FPA ratio 0.6 and the minimum is 89% at FPA ratio equal to 1.5. Thus, there is an approximately 9% reduction in the total losses in the coupled system at FPA ratio equal to 0.6, and 11% reduction at FPA ratio equals to 1.5.

With these optimization results, design engineer can select suitable core dimensions for low loss and high efficiency. Fig. 8 shows the plot of optimization results showing the reduction in loss ratio with the variation of foot print area ratio.

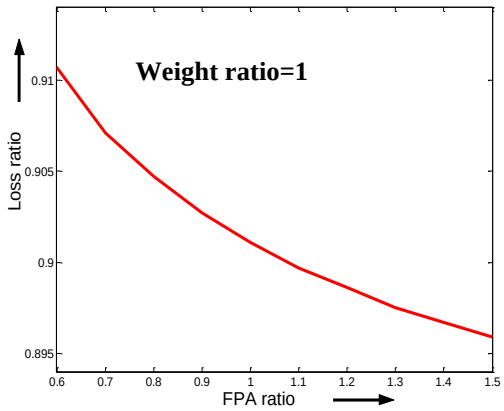

Fig. 8: Loss ratio reduction with variation of foot print area ratio

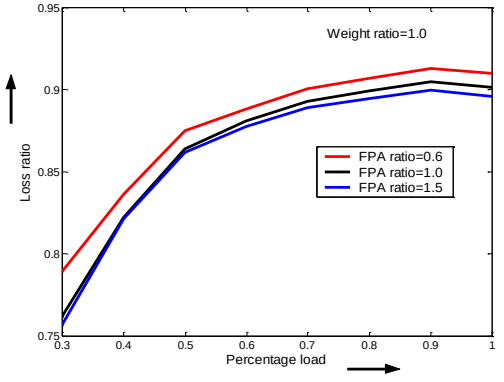

Fig. 9. Loss ratio variation with change in load for different FPA ratio.

Fig.9: shows the plot of loss ratio estimated against percentage loads for different foot print area ratio.

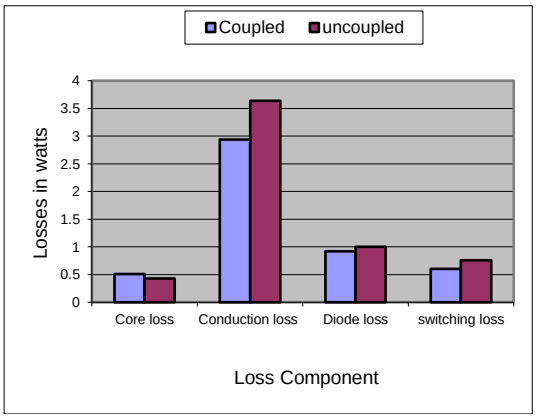

Fig. 10: Loss components in uncoupled and coupled converters

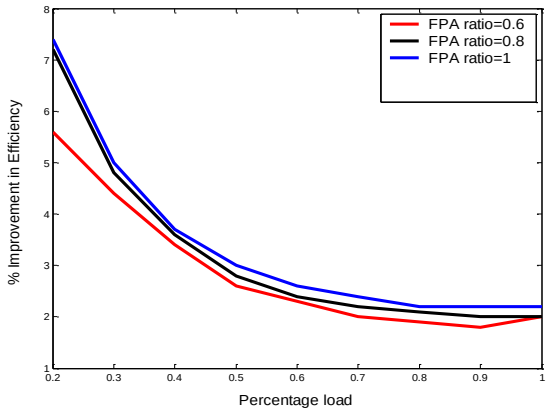

Fig. 11: Improvement in efficiency with variation of loads for different FPA ratio

From the plots it is clear that, for the entire load range the loss ratio is less than unity for small foot print area ratio. Thus, by using coupled inductor, double advantage of having less loss and less foot print area as compared to uncoupled multiphase buck converter can be achieved. Fig. 10 shows the loss components in uncoupled and coupled converters at full load.

Fig.11 shows the simulation plots of improvement in efficiency against percentage loads for different FPA ratio

Similarly, Fig. 12 shows the comparison of simulated and experimentally obtained loss ratios versus percentage loads at FPA ratio=1.

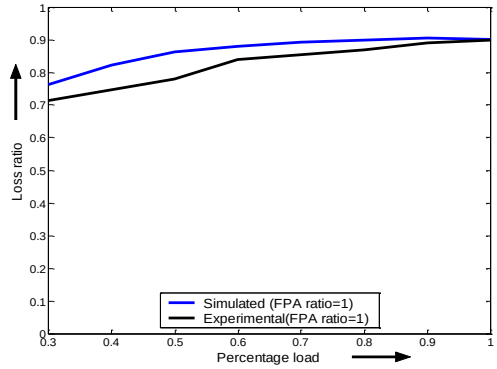

Fig. 12. Comparison of simulated and experimental results of loss ratio

Figure 13 shows the plot of Efficiency improvement in coupled system at different FPA ratios.

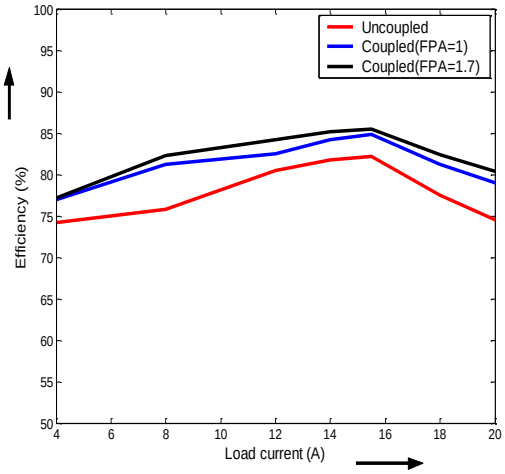

Fig. 13. Improvement in efficiency with variation of FPA ratio

VI. Conclusion

In this paper, we have presented the design and optimization of the coupled core topology for a multiphase synchronous buck converter. It is shown that, by going for coupling, total losses can be minimized. A new core structure with common leakage path and air gap adjusts the Ampere-turn requirements and minimizes the phase ripples to a greater extent. Hence, by going for this type of structure and by selecting a high permeability material, a minimum of 10% loss reduction can be achieved. Thus, an overall efficiency of 2% to 4% can be predicted with this much loss reduction. However, by experiment, we have proved that, by using coupled inductor topology, 3-4% efficiency can be improved as compared to uncoupled converter system. As we can predict the efficiency with loss estimation technique, this approach helps the design engineer in selecting the material and the size of the core. Experimentally, it is also shown that the loss components in coupled converter are less as compared to uncoupled converter.

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Design of Embedded Controller for Various Multilevel Inverter Topologies

C.R.Balamurugan [1] S.P.Natarajan [2] R.Bensraj [3]

***Abstract*– Multilevel inverter technology is an emerging trend for the control of electric drives in hybrid electric vehicles of high power rating. This paper proposes three different types of multilevel inverter topologies they are five level flying capacitor multilevel inverter, six switch hybrid multilevel inverter and five switch hybrid multilevel inverter. This paper analyses the total harmonic distortion of the chosen three types of multilevel inverter topologies. Embedded switching pattern scheme is used to improve the performance of Multilevel Inverter. For this type of inverters pulses are developed by using the embedded controller. This scheme reduces the switching loss. The proposed inverter can synthesize high quality output voltage near to sinusoidal waves. To validate the developed technique simulations are carried out through MATLAB/SIMULINK.**

Keywords– THD, FCMLI, CMLI, Embedded controller

I. INTRODUCTION

Multilevel inverters (MLI) are plays an important role in industrial power applications. Generally conventional MLIs are categorized into diode clamped, flying capacitor and Cascaded H bridge type. Conventional inverters can either produce the output levels as zero or maximum. So it is called a two level inverter. For a high power application, these types of inverters are not used. Because of it consists of losses with ripple content, frequency deviations, switching losses and device ratings. Multilevel Inverters are tremendously interest to use in Power inverters. The basic concept of a multilevel inverter is to achieve high power by using a series of power semiconductor switches with several lower DC voltage sources to perform the power conversion by synthesizing a staircase voltage waveform. Embedded Controllers (ECs) are often found in low power embedded reference designs, performing a range of input/output and system management functions. Embedded controller is a special purpose controller that is embedded in an electronic system. Embedded controllers has major role in modern machine and automobile than power control systems. Embedded controllers are often the heart of an industrial control system or a process control application. Krishna Kumar et al [1] proposed a multilevel inverter topology with input DC sources which are connected in opposite polarities with one another through power switches. This approach results in reduced number of power switches as compared to classical topologies. K.Gobinath et al [2] developed a novel cascaded multilevel inverter for harmonic elimination. Jacob James Nedumgatt et al [3] discussed a new topology of a cascaded multilevel inverter that utilizes less number of switches than the conventional topology.

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[1] Department of Electrical Engineering, Arunai Engineering College, India. E-mail: crbalain2010@gmail.com

[2] Department of EIE & EEE, Annamalai University, India. E-mail: spn_annamalai@rediffmail.com

Javad Ebrahimi et al [4] suggested a topology which reduces the number of DC voltage sources, switches as the number of output voltage levels increases. Ehsan Najafi et al [5] presented a new topology with a reversing voltage component is proposed to improve the multilevel performance. Roshankumar et al [6] developed a topology which is obtained by cascading a three-level flying capacitor inverter with a flying H-bridge power cell in each phase. K.K. Gupta et al [7] developed a topology for multilevel inverters which increases the number of levels as number of switches and conduction losses can be reduced. Ahmed et al [8] presented two types of multilevel inverters with reduced number of switches, losses. G.S. Konstantinou et al [9] proposed a topology which is a cascaded connection of a conventional three phase, two level inverter. Arif Al-Judi et al [10] proposed a Cascaded Multilevel Inverter with reduced number of Switches. Tehrani et al [11] proposed a new multilevel inverter topology. Ceglia et al [12] suggested a new inverter topology using an auxiliary switch which reducing the number of power devices required to implement a multilevel output. Leon M et al [13] proposed a multilevel inverter using carrier based PWM methods. G.Carrara et al [14] developed a multilevel inverter based on PWM method. N.S.Choi et al [15] proposed multilevel inverter that can realize any pulse width modulation scheme which leads to harmonic reduction.

II. MULTILEVEL INVERTERS

A Multilevel inverter is a power electronic device built to synthesize a desired A.C voltage from several levels of DC voltages. Multilevel inverters have gained more attention in high power applications because it has got many advantages. It can realize high voltage and high power output by using semiconductor switches without the use of transformer and dynamic voltage balance circuits. The proposed scheme is simulated under the MATLAB/SIMULINK environment. Filter is not used at the output side so the THD (Total Harmonic Distortion) is more. If small size filter is used across the load the THD will be within the IEEE standard. The another way to reduce the THD is by increasing the number of levels of the inverter. The Powergui block allows you to choose one of the following methods to solve your circuit (i) Continuous, which uses a variable step solver from Simulink (ii) Ideal Switching continuous (iii) Discretization of the electrical system for a solution at fixed time steps and (iv)Phasor solution. The Powergui block is necessary for simulation of any Simulink model containing Sim Power Systems blocks. It is used to store the equivalent SIMULINK circuit that represents the state-space equations of the model. When using this block in a model, you must follow these rules: Place the Powergui block at the top level of diagram for optimal performance. You can place it anywhere inside subsystems for your convenience; its functionality will not be affected. You can have a maximum of one

Powergui block per model. You must name the block powergui. The Powergui block also gives you access to various Graphical User Interface (GUI) tools and functions for the steady-state analysis of Sim Power Systems models, the analysis of simulation results, and for the design of advanced block parameters. In this continuous block is chosen in the powergui block.

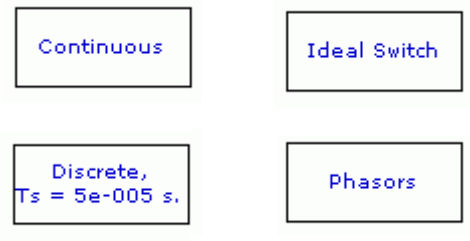

Fig. 1: Environment block for simpowersystems models (Powergui)

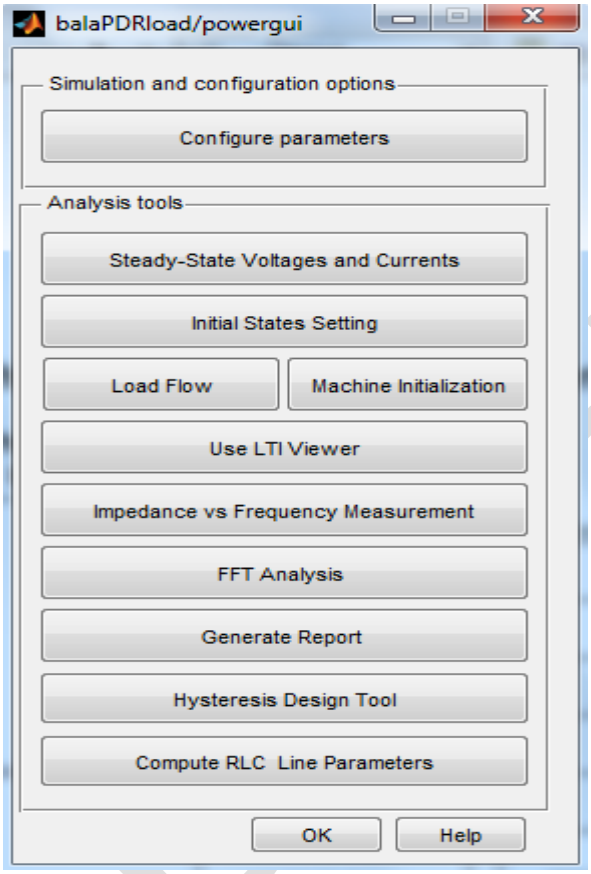

Fig. 2: Options available in the Powergui tool

A. Five Level Flying Capacitor Multilevel Inverter

The structure of this flying capacitor inverter is similar to that of the diode clamped inverter except that instead of using clamping diodes, the inverter uses capacitors in their place. The flying capacitor involves series connection of capacitor clamped switching cells. The Flying Capacitor (FC)MLI topology has a ladder structure of DC side capacitors, where the voltage on each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform. The main advantage of flying capacitor multilevel inverter is large amounts of storage capacitors can provide capabilities during power outages and also these inverters can provide switch combination redundancy for balancing different voltage levels. The input voltage value of this proposed system is V_{dc}=200 V and the load R=100ohms.

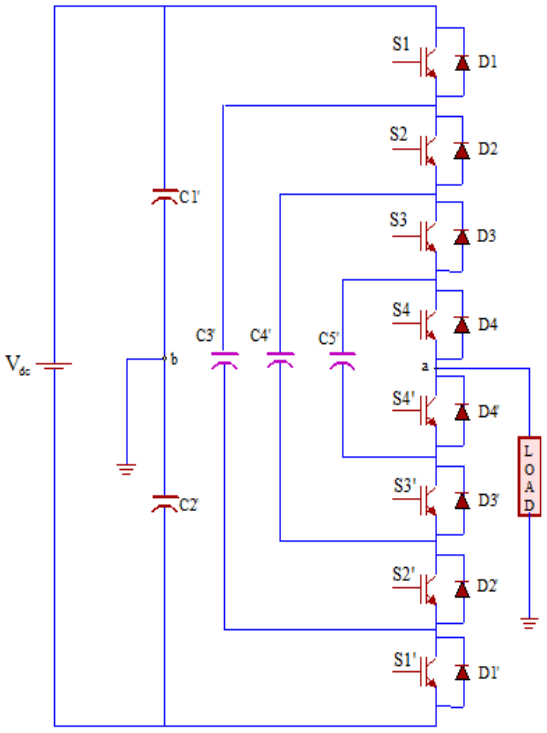

Fig.3: Half bridge five level flying capacitor inverter for R-phase

Fig.3 shows the general structure of half bridge five level flying capacitor inverter for R-phase. FCMLI requires 8 semiconductor switches (S1-S4, S1'-S4') 3 flying capacitors (C3', C4', C5') and 2 DC link capacitors (C1', C2'). This FCMLI consists of four switch pairs (S1,S1'), (S2,S2'), (S3,S3') and (S4,S4'). The switches are clamped by DC-link together with flying capacitors. The four switches (S1-S4) must be connected in series between DC input and load and likewise for switches (S4'-S1'). The three flying capacitors C3', C4' and C5' are charged to different voltage levels. By changing the transistor switching states, the capacitors and the DC source are connected in different ways to produce different load voltage levels. A typical switch combination used to synthesize the various load voltages are shown in Table 1.
This proposed five level flying capacitor multilevel inverter consists of eight switching devices. The switching states of the multilevel inverter are given as the input for the embedded controller based proposed system. This proposed system provides the five output level $+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$, $-2V_{dc}$. At the level of $2V_{dc}$, the first four switches should be turn ON and the remaining switches will be turned OFF. In the $+V_{dc}$ level P1, P2, P3, P5 switches will be turned ON. At the level of 0Vdc P1, P2, P5, P6 should be turned ON. The $-V_{dc}$ level contains P1, P5, P6, P7 will be turned ON. At the level of $-2V_{dc}$ the lower four switches should be turned ON. This proposed system used to obtain the five level output, which are nearer to the sinusoidal output. This proposed system is used to reduce the THD and it can be used to increase the performance of the system. It also can be used to reduce

the switching losses. The schematic diagram of proposed method is shown in the Fig. 3.

Table 1 : Switching states of five-level flying capacitor multilevel inverter

S1	S2	S3	S4	C3'	C4'	C5'	V_{ab}
1	1	1	1	NC	NC	NC	$+V_{dc}/2$
1	1	1	0	NC	NC	+	
1	1	0	1	NC	+	-	$+V_{dc}/4$
1	0	1	1	+	-	NC	
0	1	1	1	-	NC	NC	
0	0	1	1	NC	-	NC	
0	1	0	1	-	+	-	
0	1	1	0	-	NC	+	0
1	0	0	1	+	NC	-	
1	0	1	0	+	-	+	
1	1	0	0	NC	+	NC	
1	0	0	0	+	NC	NC	
0	1	0	0	-	+	NC	
0	0	1	0	NC	-	+	$-V_{dc}/4$
0	0	0	1	NC	NC	-	
0	0	0	0	NC	NC	NC	$-V_{dc}/2$

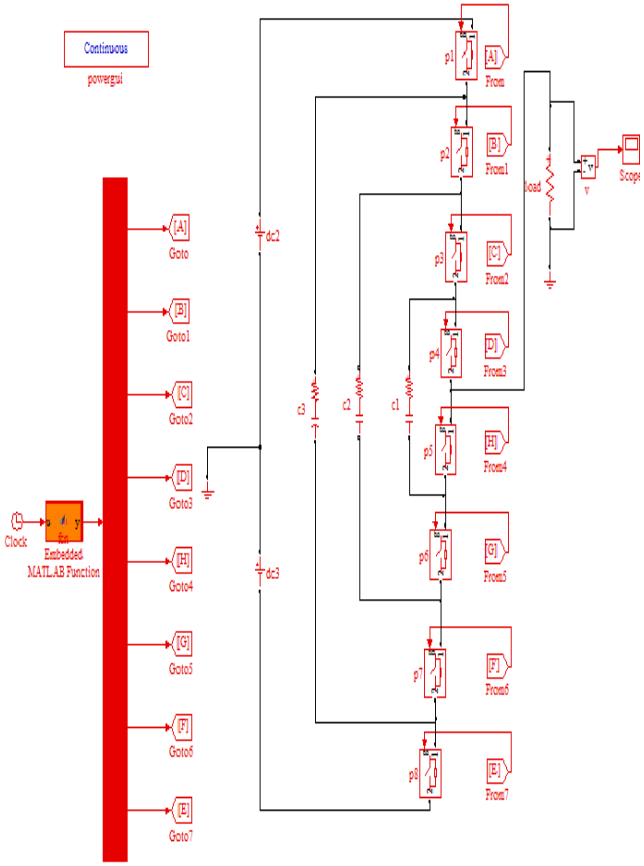

Fig. 4: Sample simulation circuit of five level flying capacitor multilevel inverter using R load

The above table 1 represents the switching states which are given as the input for the proposed five level flying capacitor multilevel inverter. By using the embedded controller the five level output can be obtained for this proposed system. The simulation output of the proposed system is shown in Figure 5. The THD which is a measure of closeness in shape between a waveform and its fundamental component. When the voltage levels of the topologies are increases, the harmonic content of the output voltage waveform decreases significantly.

$$THD = \frac{1}{V_1}\sqrt{\sum_{n=2,3..}^{\infty} V_n^2} \quad (1)$$

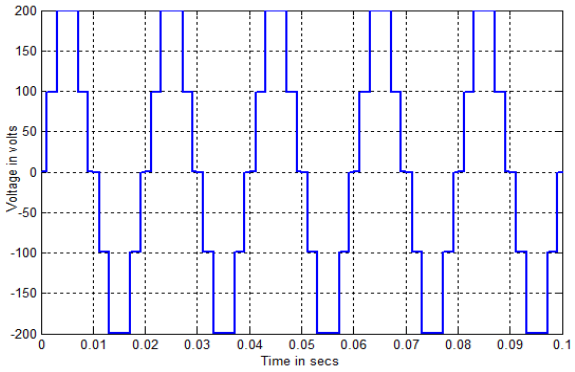

Fig. 5: Five level output voltage of FCMLI

The THD value for the proposed system is shown in Figure 6.

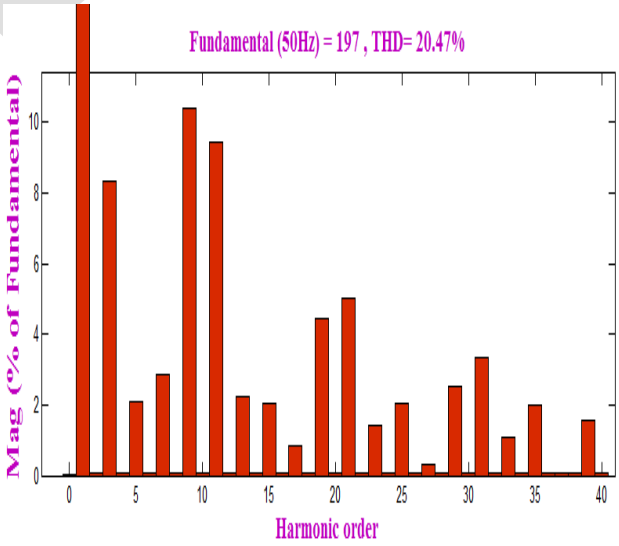

Fig. 6: FFT plot for five level output voltage

By seeing the truth table the coding are generated. This method of generation of pulses is similar to (Selective Harmonic Elimination) SHE PWM method. The coding are developed with the help of MATLAB software.

```
function y  = fcn(u)
 a = mod(u*1000,10);
b = mod(u*1000,20);
 if a<1.2 %0
    p1=1;
    p2=1;
    p3=0;
```

```
    p4=0;
    p5=1;
    p6=1;
    p7=0;
    p8=0;
elseif a<3.1 %3
    p1=1;
    p2=1;
    p3=1;
    p4=0;
    p5=1;
    p6=0;
    p7=0;
    p8=0;
 elseif a<7.2 %4
    p1=1;
    p2=1;
    p3=1;
    p4=1;
    p5=0;
    p6=0;
    p7=0;
    p8=0;
    elseif a<9.1 %5
    p1=1;
    p2=1;
    p3=1;
    p4=0;
    p5=1;
    p6=0;
    p7=0;
    p8=0;
   else %0
    p1=1;
    p2=1;
    p3=0;
    p4=0;
    p5=1;
    p6=1;
    p7=0;
    p8=0;
end
if b<10
y=[p1,p2,p3,p4,p5,p6,p7,p8];
else
y=[p5,p6,p7,p8,p1,p2,p3,p4];
end
```

B. Six Switch Hybrid Multilevel Inverter

The next proposed circuit is embedded controller based five level hybrid cascaded inverter with reduced number of switches is shown in Figure 7. Each separate voltage source V_{dc1}, V_{dc2}, V_{dc3} is connected in cascade with other sources via a special H-bridge circuit associated with it. The most important part in multilevel inverters is switches which define the reliability, circuit size, cost, installation area and control complexity. The first H-bridge circuit consists of four active switching elements and the second Voltage Source Inverter (VSI) circuit consists of two active switching elements that can make the output voltage either positive or negative polarity or it can also be simply zero volts which depends on the switching condition of switches in the circuit.

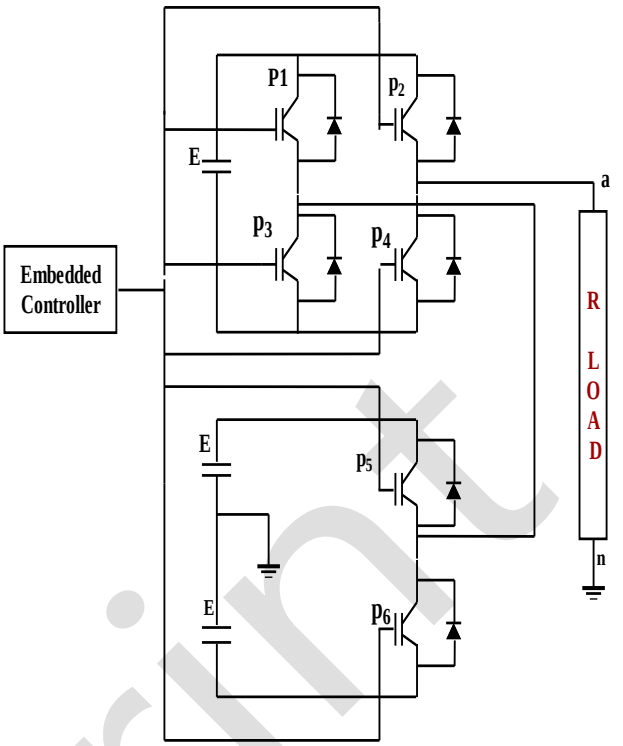

Fig. 7: Five level embedded controller based hybrid multilevel inverter

At the level of $2V_{dc}$, P2, P3, P5 switches should be turned ON. In the V_{dc} level P1, P2, P5 will be turned ON and the remaining switches will turned OFF. The $0V_{dc}$ level contains P2; P3 and P6 switches will be turned ON. At the level of $-V_{dc}$, P1, P2 and P6 switches will be turned ON and the $-2V_{dc}$ level contains P1, P4 and P6 switches should be turned ON. The advantages of cascaded multilevel inverter are modularized layout and packaging. This enables the manufacturing process to be done more quickly and cheaply. In this proposed system the switching states are given as the input by using the MATLAB/SIMULINK. The input voltage value of this proposed system is V_{dc}=200V and the load R=100ohms.

Table 2 : Switching states for five level proposed hybrid cascaded multilevel inverter

Switching states						Output Voltage
P_1	P_2	P_3	P_4	P_5	P_6	
0	1	1	0	1	0	$2V_{dc}$
1	1	0	0	1	0	V_{dc}
0	1	1	0	0	1	0
1	1	0	0	0	1	$-V_{dc}$
1	0	0	1	0	1	$-2V_{dc}$

The switching states of the proposed hybrid multilevel inverter are shown in Table 2. These switching states are given as the input and the proposed system produce the five levels of output. The simulation output of hybrid multilevel inverter is shown in Figure 8.

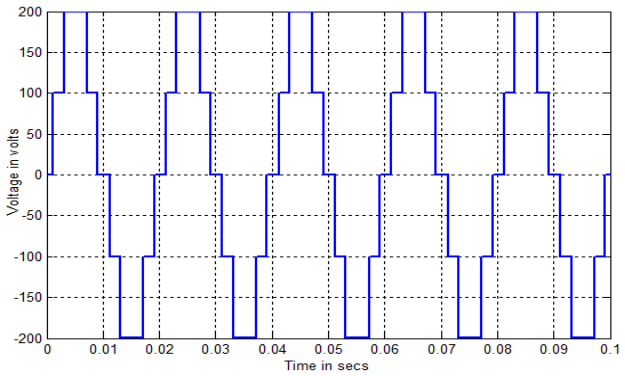

Fig. 8: Simulation output of proposed hybrid multilevel inverter

The total harmonic distortion of the proposed system is shown in Figure 9.

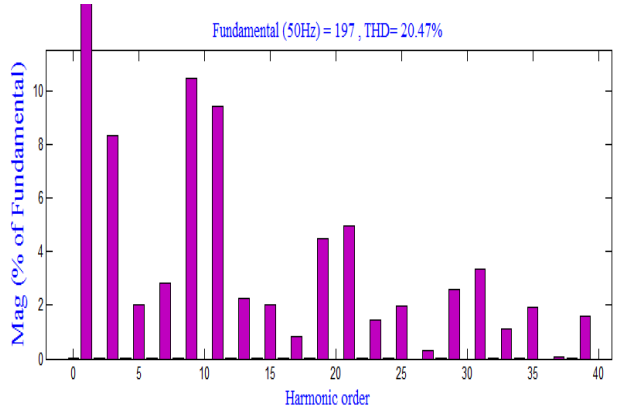

Fig. 9: THD plot for proposed hybrid multilevel inverter

The coding for six switch hybrid MLI is given below

```
function y  = fcn(u)
 a = mod(u*1000,10);
b = mod(u*1000,20);
if a<1.2 %0
    p1=0;
    p2=1;
    p3=1;
    p4=0;
    p5=0;
    p6=1;
elseif a<3.1 %1
    p1=1;
    p2=1;
    p3=0;
    p4=0;
    p5=1;
    p6=0;
 elseif a<7.2 %2
    p1=0;
    p2=1;
    p3=1;
    p4=0;
    p5=1;
    p6=0;
elseif a<9.1 %1
    p1=1;
    p2=1;
    p3=0;
    p4=0;
    p5=1;
    p6=0;
else  %0
     p1=0;
    p2=1;
    p3=1;
    p4=0;
    p5=0;
    p6=1;
 end
if b<10
y=[p2,p3,p5,p1,p4,p6];
else
y=[p1,p4,p6,p2,p3,p5];
end
```

C. Five Switch Hybrid Multilevel Inverter

The next proposed hybrid multilevel inverter is shown in figure 10. This type of proposed system contains five switches which produce the five levels of output by using the embedded controller based MATLAB/SIMULINK. The input voltage value of this proposed system is V_{dc}=200V and the load R=100ohms.

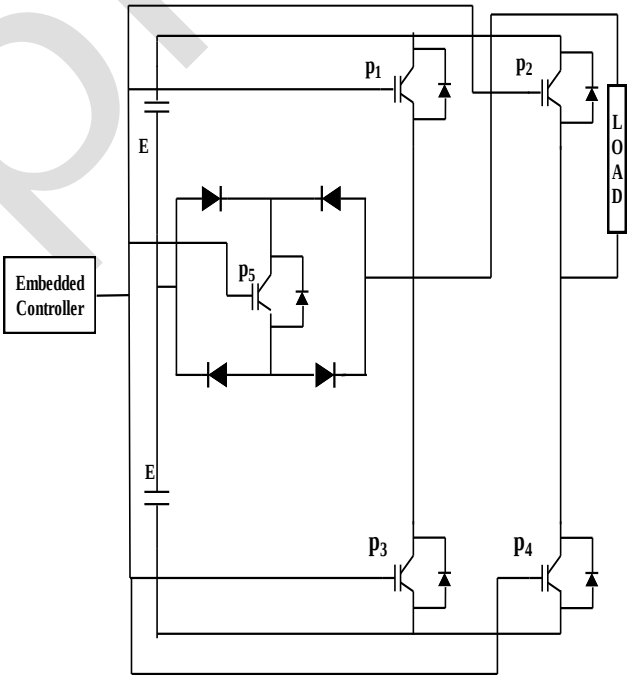

Fig. 10: Five level Embedded controller based hybrid multilevel inverter

This proposed system contains five switches which produce the desired five level output. At the level of $+2V_{dc}$, P1 and P4 switches should be turned ON and the remaining switches will be turned OFF. In the $+V_{dc}$ level P4 and P5 will be turned ON. The 0Vdc level contains P2 and P4 switches will be turned ON. At the level of $-V_{dc}$, P3 and P5 switches will be turned ON and the $-2V_{dc}$ level contains P2 and P3 switches should be turned ON. The switching states of the above proposed system are shown in Table 3.

Table 3: Switching states for embedded controller based hybrid multilevel inverter

Switching states					Output voltage
P_1	P_2	P_3	P_4	P_5	
1	0	0	1	0	$2V_{dc}$
0	0	0	1	1	V_{dc}
0	1	0	1	0	0
0	0	1	0	1	$-V_{dc}$
0	1	1	0	0	$-2V_{dc}$

By using these switching states the Hybrid MLI can produce five levels of output. The simulation output of the proposed system is shown in Figure 11.

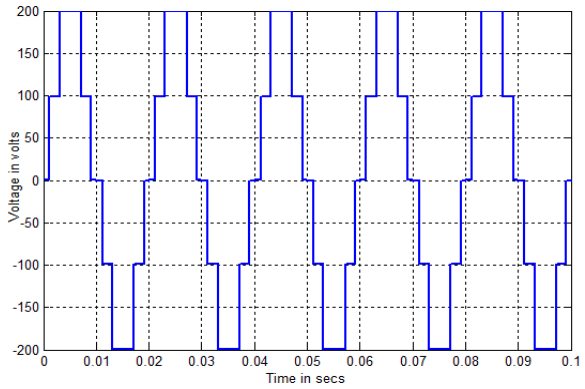

Fig. 11: Simulation output of embedded controller based hybrid multilevel inverter

The total harmonic distortion of the proposed five level hybrid multilevel inverter is shown in Figure 12.

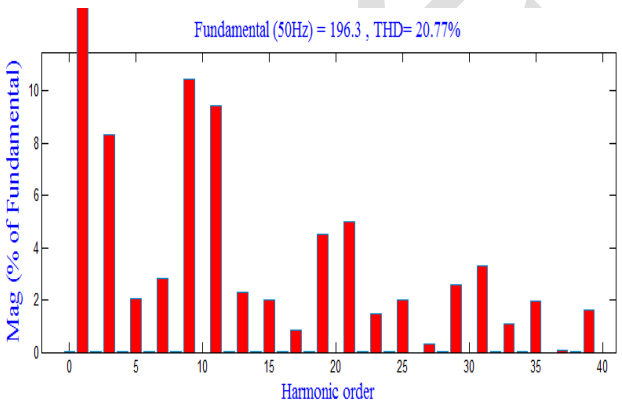

Fig. 12: THD plot for Embedded Controller based hybrid multilevel inverter

The program for the five switch MLI is given below

```
function y  = fcn(u)
a = mod(u*1000,10);
b = mod(u*1000,20);
if a<1.2 %0
   p1=0;
   p2=1;
   p3=0;
   p4=1;
   p5=0;
elseif a<3.1 %1
   p1=0;
   p2=0;
   p3=0;
   p4=1;
   p5=1;
 elseif a<7.2 %2
    p1=1;
   p2=0;
   p3=0;
   p4=1;
   p5=0;
 elseif a<9.1 %1
   p1=0;
   p2=0;
   p3=0;
   p4=1;
   p5=1;
  else %0
   p1=0;
   p2=1;
   p3=0;
   p4=1;
   p5=0;
end
if b<10
y=[p1,p4,p2,p3,p5];
else
y=[p2,p3,p1,p4,p5];
end
```

In a Direct Current (DC) circuit, voltage or current is simple to define, but in an Alternating Current (AC) circuit, the definition is more complicated, and can be done in several ways. Root Mean Square (RMS) refers to the most common mathematical method of defining the effective voltage or current of an AC wave. The number of pulses p per half cycle depends on the carrier frequency. By varying the modulation index m_a, the RMS output voltage can be varied. The area of each pulse corresponds approximately to the area under the sine wave between the adjacent midpoints of off periods on the gating signals. If δ_m is the width of the m^{th} pulse, the RMS output voltage can be expressed as follows:

$$V_{RMS} = V_{dc}\sqrt{\sum_{m=1}^{2p}\frac{\delta_m}{\pi}} \qquad (2)$$

Table 4 shows the output obtained for the three topologies chosen. Comparing the different topology of 5-level inverter it is observed that 5-level hybrid five switch MLI requires lesser number of switches. But comparing the performance of the different topology almost three of the MLI provides similar performance only. In the case of five levels hybrid six switches MLI is the combination of H-bridge and VSI inverter. The H-bridge and Voltage source inverter produce 3-levels. These two circuits are connected in series so total output is five levels. In five levels hybrid five switches MLI is the combination of H-bridge and Diode bridge rectifier with one switch. Both circuits produce three levels. By adding five level is obtains as a final output. To implement the inverter it is possible select the Field Programmable Gate Array (FPGA)/dSPACE to generate gate pulse for the switches used. Power circuits are developed with Power (Metal Oxide Semiconductor

Field Effect Transistor) MOSFET and Power diodes. The voltage sources used for hardware may be from battery or through solar panels. Control circuit consists of MOSFET driver circuit, opto coupler and FPGA/dSPACE controller.

Table 4: Parameters of three proposed topologies

Topology	Number of switches	THD	V_{rms}
5-Level FCMLI	8	20.47%	197
5-Level Hybrid six switch MLI	6	20.47%	197
5-Level Hybrid five switch MLI	5	20.77%	196.3

Table 5: Comparison of power component requirement for the chosen inverters

Topology	5-Level FCMLI	5-Level Hybrid 6-switch MLI	5-Level Hybrid 5-switch MLI
Main Switching devices	8	6	5
Main diodes	8	6	10
Clamping capacitors	12	-	-
DC bus Capacitors	4	-	-
DC voltage sources	1	3	2

III. Conclusion

In these paper three types of embedded controller based multilevel inverter topologies are proposed. The topologies are five level flying capacitor multilevel inverter, six switch five level hybrid multilevel inverter and five switch hybrid MLI topologies. The most important feature of the hybrid multilevel inverter is being convenient for expanding and increasing the number of output levels simply with less number of switches. The switching losses also reduced and the performance of the system will be increased. The total harmonic distortion value of the embedded controller based proposed topologies are reduced than the conventional topologies. The total harmonic distortion value of proposed topologies is 20.47%, 20.47% and 20.77%.

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Biographies

Dr. C.R.Balamurugan was born in 1978 in Kumbakonam. He has obtained B.E (Electrical and Electronics), M.E (Power Electronics and Drives) degree and Ph.D (MultiLevel Inverters) in 2000, 2005 and 2015 respectively from Arunai Engineering College, Tiruvannamalai, Sathyabama University, Chennai and Annamalai University, Chidambaram. He has been working in the teaching field for about 12 years. His areas of interest include power electronics, electrical machines and solar energy systems. He has 60 publications in international journals. His research papers 50 have been presented in various/IEEE international/national conferences. Currently, he is working as Associate Professor in the Department of EEE, Arunai Engineering College, Tiruvannamalai. He is a life member of Instrument Society of India and Indian Society for Technical Education. Contact number- +91-9894522351. E-mail:crbalain2010@gmail.com.

Dr. S.P.Natarajan was born in 1955 in Chidambaram. He has obtained B.E (Electrical and Electronics) and M.E (Power Systems) degrees in

1978 and 1984 respectively from Annamalai University securing distinction and then Ph.D in Power Electronics from Anna University, Chennai in 2003. He is Former Professor and Head of Instrumentation Engineering Department at Annamalai University where he has put in 31 years of service. He produced eight Ph.Ds and presently guiding eight Ph.D Scholars and so far guided eighty M.E students. His research papers 66 have been presented in various/IEEE international/national conferences in Mexico, Virginia, Hong Kong, Malaysia, India, Singapore and Korea. He has 20 publications in national journals and 100 in international journals. His research interests are in modeling and control of DC-DC converters and multiple connected power electronic converters, control of permanent magnet brushless DC motor, embedded control for multilevel inverters and matrix converters etc. He is a life member of Instrument Society of India and Indian Society for Technical Education. Contact number- +91-9443185211. Email: spn_annamalai@rediffmail.com.

Dr.R.Bensraj was born in 1973 in Marthandam. He has obtained B.E (Electrical and Electronics), M.E (Power Systems) and Ph.d (Multilevel Inverter) degrees from Annamalai University, Chidambaram. He has been working in the teaching field for about 13 years. His areas of interest include power electronics, electrical machines and solar energy systems. He has 32 publications in international journals. His research papers 10 have been presented in various/IEEE international/national conferences. Currently, he is working as Associate Professor in the Department of EEE, Annamalai University, Chidambaram. He is a life member of Indian Society for Technical Education. Contact number- +91-9443929992. E-mail:bensraj_au@rediffmail.com.

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